should be preferred in Figure 6-3, since the active levels of the ’151 inputs and outputs would then match their signal names. However, in data transfer and storage applications, designers (and the book) don’t always “go by the book.” It is usually clear from the context that a multiplexer (or a multibit register, in Section 8.2.5) does not alter the active level of its data.

6.1.3 Dual-Priority Encoder

Quite often MSI building blocks need a little help from their friends—ordinary gates— to get the job done. In this example, we’d like to build a priority encoder that identifies not only the highest but also the second-highest priority asserted signal among a set of eight request inputs.

We’ll assume for this example that the request inputs are active low and are named R0_L–R7_L, where R0_L has the highest priority. We’ll use A2–A0 and AVALID to identify the highest-priority request, where AVALID is asserted only if at least one request input is asserted. We’ll use B2–B0 and BVALID to identify the second-highest-priority request, where BVALID is asserted only if at least two request inputs are asserted.

Finding the highest-priority request is easy enough, we can just use a 74x148. To find the second highest-priority request, we can use another ’148, but only if we first “knock out” the highest-priority request before applying the request inputs. This can be done using a decoder to select a signal to knock out, based on A2–A0 and AVALID from the first ’148. These ideas are combined in the solution shown in Figure 6-6. A 74x138 decoder asserts at most one of its eight outputs, corresponding to the highest-priority request input. The outputs are fed to a rank of NAND gates to “turn off” the highest-priority request.

A trick is used in this solution is to get active-high outputs from the ’148s, as shown in Figure 6-5. We can rename the address outputs A2_L–A0_L to be active high if we also change the name of the request input that is associated with each output combination. In particular, we complement the bits of the request number. In the redrawn symbol, request input I0 has the highest priority.

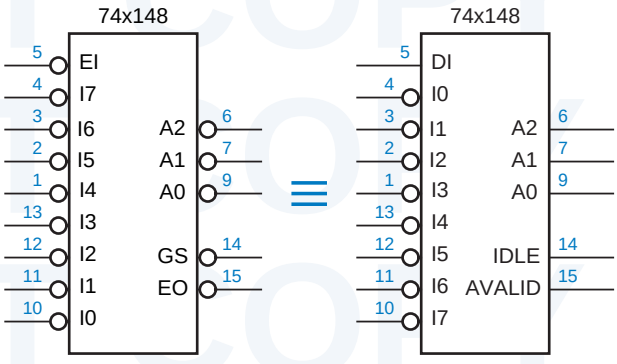

Figure 6-5
Alternate logic symbols for the 74x148 8-input priority encoder.

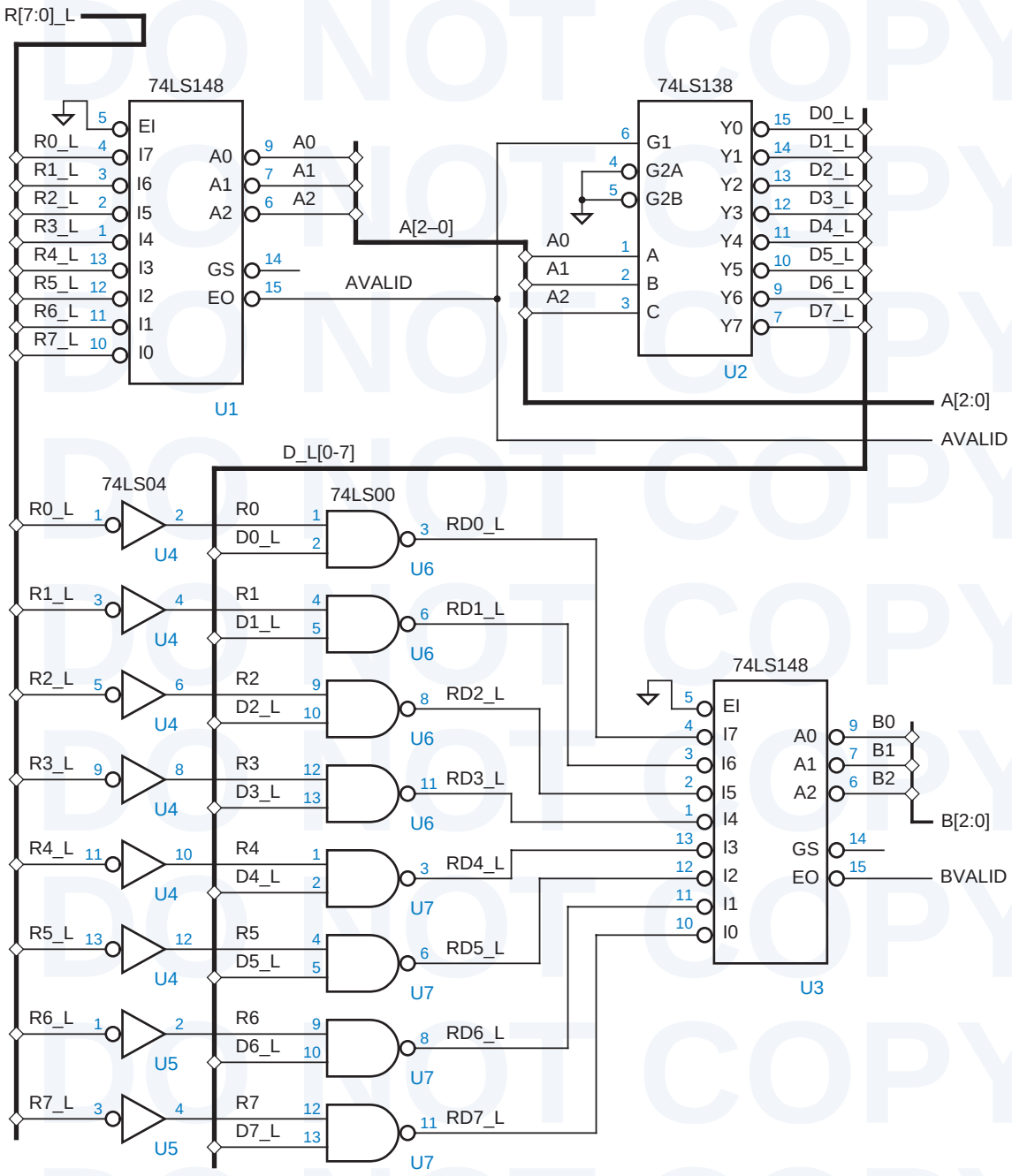

Figure 6-6 First-and second-highest priority encoder circuit.