S	CLK D = 00	CLK D = 01	CLK D = 11	CLK D = 10
SB	(SB) , 01	S6 , 01	(SB) , 01	(SB) , 01
S3	(S3) , 10	S7 , 10	— , –	SB , 01
S6	SB , 01	(S6) , 01	S7 , 11	— , –
S7	S3 , 10	(S7) , 10	(S7) , 10	(S7) , 10
	S* , Q			QN

Figure 7-74
Reduced flow and output table for a positive edge-triggered D flip-flop.

internal state S2 or S6, depending on whether D was 0 or 1 at the time; but still the output is unchanged. Once again, we can change D between 0 and 1 as much as we want, this time bouncing between S2 and S6 without changing the output.

The moment of truth finally comes when CLK changes to 1. Depending on whether we are in S2 or S6, we go back to S0 (leaving Q at 0) or to S7 (setting Q to 1). Similar behavior involving S3 and S7 can be observed on a rising clock edge that causes Q to change from 1 to 0.

In Figure 7-19, we showed a circuit for a positive edge-triggered D flip-flop with only two feedback loops and hence four states. The circuit that we just analyzed has three loops and eight states. Even after eliminating unused states, the flow table has five states. However, a formal state-minimization procedure can be used to show that states S0 and S2 are "compatible," so that they can be merged into a single state SB that handles the transitions for both original states, as shown in Figure 7-74. Thus, the job really could have been done by a four-state circuit. In fact, in Exercise 7.49 you'll show that the circuit in Figure 7-19 does the job specified by the reduced flow table.

*7.5.5 CMOS D Flip-Flop Analysis

CMOS flip-flops typically use transmission gates in their feedback loops. For example, Figure 7-75 shows the circuit design of the "FD1" positive-edge-triggered D flip-flop in LSI Logic's LCA10000 series of CMOS gate arrays. Such a flip-flop can be analyzed in the same way as a purely logic-gate based design, once you recognize the feedback loops. Figure 7-75 has two feedback loops, each of which has a pair of transmission gates in a mux-like configuration controlled by CLK and CLK′, yielding the following loop equations:

$$Y1* = CLK' \cdot D' + CLK \cdot Y1$$
$$Y2* = CLK \cdot Y1' + CLK' \cdot Y2$$

Except for the double inversion of the data as it goes from D to Y2∗ (once in the Y1∗ equation and again in the Y2∗ equation), these equations are very reminiscent of the master/slave-latch structure of the D flip-flop in Figure 7-15.

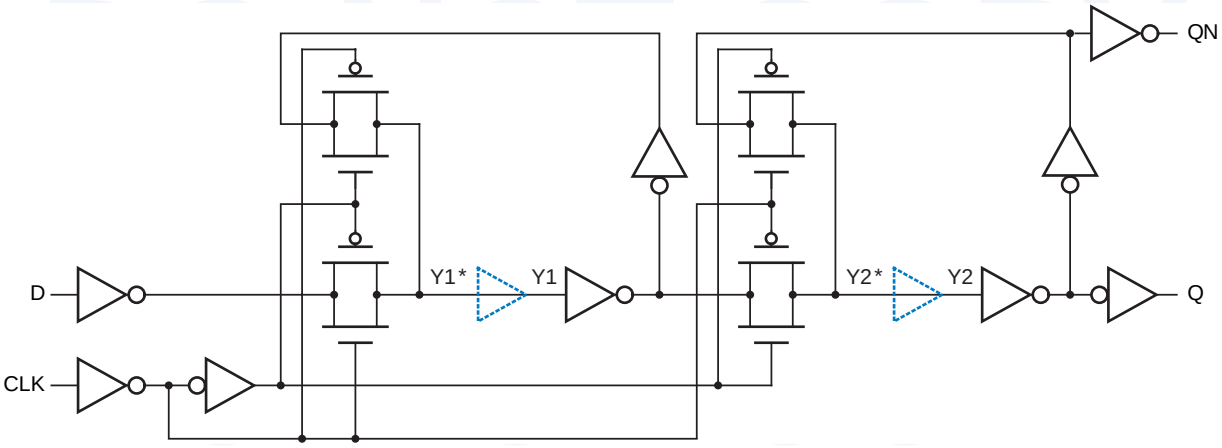

Figure 7-75 Positive edge-triggered CMOS D flip-flop for analysis.

Completing the formal analysis of the circuit is left as an exercise (7.56). Note, however, that since there are just two feedback loops, the resulting state and flow tables will have the minimum of just four states.

FEEDBACK CIRCUIT DESIGN

The feedback sequential circuits that we've analyzed in this section exhibit quite reasonable behavior since, after all, they are latch and flip-flop circuits that have been used for years. However, if we throw together a "random" collection of gates and feedback loops, we won't necessarily get "reasonable" sequential circuit behavior. In a few rare cases, we may not get a sequential circuit at all (see Exercise 7.50), and in many cases, the circuit may be unstable for some or all input combinations (see Exercise 7.55). Thus, the design of feedback sequential circuits continues to be something of a black art, and is practiced only by a small fraction of digital designers. Still, the next section introduces basic concepts that help you do simple designs.

*7.6 Feedback Sequential Circuit Design

It's sometimes useful to design a small feedback sequential circuit, such as a specialized latch or a pulse catcher; this section will show you how. It's even possible that you might go on to be an IC designer, and be responsible for designing high-performance latches and flip-flops from scratch. This section will serve as an introduction to the basic concepts you'll need, but you'll still need considerably more study, experience, and finesse to do it right.

*7.6.1 Latches

Although the design of feedback sequential circuits is generally a hard problem, some circuits can be designed pretty easily. Any circuit with one feedback loop