

**Table 3-13** Manufacturers' logic data books.

<i>Manufacturer</i>	<i>Order Number</i>	<i>Topics</i>	<i>Title</i>	<i>Year</i>
Texas Instruments	SDLD001	74, 74S, 74LS TTL	<i>TTL Logic Data Book</i>	1988
Texas Instruments	SDAD001C	74AS, 74ALS TTL	<i>ALS/AS Logic Data Book</i>	1995
Texas Instruments	SDFD001B	74F TTL	<i>F Logic Data Book</i>	1994
Texas Instruments	SCLD001D	74HC, 74HCT CMOS	<i>HC/HCT Logic Data Book</i>	1997
Texas Instruments	SCAD001D	74AC, 74ACT CMOS	<i>AC/ACT Logic Data Book</i>	1997
Texas Instruments	SCLD003A	74AHC, 74AHCT CMOS	<i>AHC/AHCT Logic Data Book</i>	1997
Motorola	DL121/D	74F, 74LSTTL	<i>Fast and LSTTL Data</i>	1989
Motorola	DL129/D	74HC, 74HCT	<i>High-Speed CMOS Data</i>	1988
Motorola	DL138/D	74AC, 74ACT	<i>FACT Data</i>	1988
Motorola	DL122/D	10K ECL	<i>MECL Device Data</i>	1989

by Howard Johnson and Martin Graham (Prentice Hall, 1993). It combines solid electronics principles with tremendous insight and experience in the design of practical digital systems.

Characteristics of today's logic families can be found in the data books published by the device manufacturers. Both Texas Instruments and Motorola publish comprehensive data books for TTL and CMOS devices, as listed in Table 3-13. Both manufacturers keep up-to-date versions of their data books on the Web, at [www.ti.com](http://www.ti.com) and [www.mot.com](http://www.mot.com). Motorola also provides a nice introduction to ECL design in the *MECL System Design Handbook* (publ. HB205, rev. 1, 1988).

The JEDEC (Joint Electron Device Engineering Council) standards for digital logic levels can be found on JEDEC's Web site, [www.jedec.org](http://www.jedec.org). The JEDEC standards for 3.3-V, 2.5-V, and 1.8-V logic were published in 1994, 1995, and 1997, respectively.

## Drill Problems

- 3.1 A particular logic family defines a LOW signal to be in the range 0.0–0.8 V and a HIGH signal to be in the range 2.0–3.3 V. Under a positive-logic convention, indicate the logic value associated with each of the following signal levels:
- (a) 0.0 V    (b) 3.0 V    (c) 0.8 V    (d) 1.9 V  
 (e) 2.0 V    (f) 5.0 V    (g) –0.7 V    (h) –3.0 V
- 3.2 Repeat Drill 3.1 using a negative-logic convention.
- 3.3 Discuss how a logic buffer amplifier is different from an audio amplifier.

- 3.4 Is a buffer amplifier equivalent to a 1-input AND gate or a 1-input OR gate?
- 3.5 True or false: For a given set of input values, a NAND gate produces the opposite output as a NOR gate.
- 3.6 Write two completely different definitions of “gate” used in this chapter.
- 3.7 What kind of transistors are used in CMOS gates?
- 3.8 (Hobbyists only.) Draw an equivalent circuit for a CMOS inverter using a single-pole, double-throw relay.
- 3.9 For a given silicon area, which is likely to be faster, a CMOS NAND gate or a CMOS NOR?
- 3.10 Define “fan-in” and “fanout.” Which one are you likely to have to calculate?
- 3.11 Draw the circuit diagram, function table, and logic symbol for a 3-input CMOS NOR gate in the style of Figure 3-16.
- 3.12 Draw switch models in the style of Figure 3-14 for a 2-input CMOS NOR gate for all four input combinations.
- 3.13 Draw a circuit diagram, function table, and logic symbol for a CMOS OR gate in the style of Figure 3-19.
- 3.14 Which has fewer transistors, a CMOS inverting gate or a noninverting gate?
- 3.15 Name and draw the logic symbols of four different 4-input CMOS gates that each use 8 transistors.
- 3.16 The circuit in Figure X3.16(a) is a type of CMOS AND-OR-INVERT gate. Write a function table for this circuit in the style of Figure 3-15(b), and a corresponding logic diagram using AND and OR gates and inverters.
- 3.17 The circuit in Figure X3.16(b) is a type of CMOS OR-AND-INVERT gate. Write function table for this circuit in the style of Figure 3-15(b), and a corresponding logic diagram using AND and OR gates and inverters.
- 3.18 How is it that perfume can be bad for digital designers?

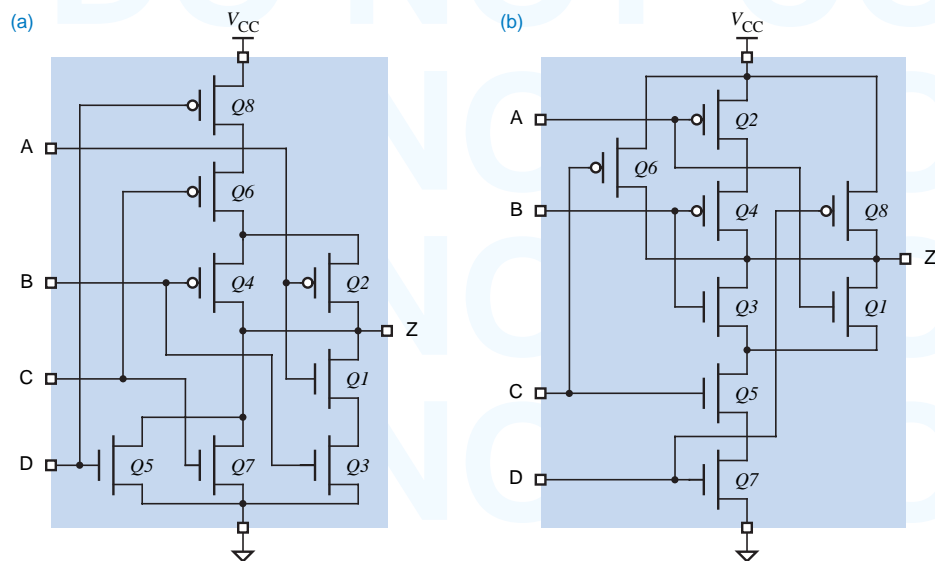


Figure X3.16

- 3.19 How much high-state DC noise margin is available in a CMOS inverter whose transfer characteristic under worst-case conditions looks like Figure 3-25? How much low-state DC noise margin is available? (Assume standard 1.5-V and 3.5-V thresholds for LOW and HIGH.)
- 3.20 Using the data sheet in Table 3-3, determine the worst-case LOW-state and HIGH-state DC noise margins of the 74HC00. State any assumptions required by your answer.
- 3.21 Section 3.5 defines seven different electrical parameters for CMOS circuits. Using the data sheet in Table 3-3, determine the worst-case value of each of these for the 74HC00. State any assumptions required by your answer.
- 3.22 Based on the conventions and definitions in Section 3.4, if the current at a device output is specified as a negative number, is the output sourcing current or sinking current?
- 3.23 For each of the following resistive loads, determine whether the output drive specifications of the 74HC00 over the commercial operating range are exceeded. (Refer to Table 3-3, and use  $V_{OHmin} = 3.84\text{ V}$  and  $V_{CC} = 5.0\text{ V}$ .)
- |                               |  |
|-------------------------------|--|
| (a) $120\ \Omega$ to $V_{CC}$ | (b) $270\ \Omega$ to $V_{CC}$ and $330\ \Omega$ to GND |
| (c) $1\text{ K}\Omega$ to GND | (d) $150\ \Omega$ to $V_{CC}$ and $150\ \Omega$ to GND |
| (e) $100\ \Omega$ to $V_{CC}$ | (f) $75\ \Omega$ to $V_{CC}$ and $150\ \Omega$ to GND  |
| (g) $75\ \Omega$ to $V_{CC}$  | (h) $270\ \Omega$ to $V_{CC}$ and $150\ \Omega$ to GND |
- 3.24 Across the range of valid HIGH input levels, 2.0–5.0 V, at what input level would you expect the 74HC00 (Table 3-3) to consume the most power?
- 3.25 Determine the LOW-state and HIGH-state DC fanout of the 74HC00 when it drives 74LS00-like inputs. (Refer to Tables 3-3 and 3-12.)
- 3.26 Estimate the “on” resistances of the  $p$ -channel and  $n$ -channel output transistors of the 74HC00 using information in Table 3-3.
- 3.27 Under what circumstances is it safe to allow an unused CMOS input to float?
- 3.28 Explain “latch up” and the circumstances under which it occurs.
- 3.29 Explain why putting all the decoupling capacitors in one corner of a printed-circuit board is not a good idea.
- 3.30 When is it important to hold hands with a friend?
- 3.31 Name the two components of CMOS logic gate’s delay. Which one is most affected by load capacitance?
- 3.32 Determine the  $RC$  time constant for each of the following resistor-capacitor combinations:
- |   |  |
|---|--|
| (a) $R = 100\ \Omega$ , $C = 50\text{ pF}$      | (b) $R = 330\ \Omega$ , $C = 150\text{ pF}$        |
| (c) $R = 1\text{ K}\Omega$ , $C = 30\text{ pF}$ | (d) $R = 4.7\text{ K}\Omega$ , $C = 100\text{ pF}$ |
- 3.33 Besides delay, what other characteristic(s) of a CMOS circuit are affected by load capacitance?
- 3.34 Explain why the number of CMOS inputs connected to the output of a CMOS gate generally is not limited by DC fanout considerations.

- 3.35 It is possible to operate 74VHC CMOS devices with a 3.3-volt power supply. How much power does this typically save, compared to 5-volt operation?
- 3.36 A particular Schmitt-trigger inverter has  $V_{ILmax} = 0.8$  V,  $V_{IHmin} = 2.0$  V,  $V_{T+} = 1.6$  V, and  $V_{T-} = 1.3$  V. How much hysteresis does it have?
- 3.37 Why are three-state outputs usually designed to turn off faster than they turn on?
- 3.38 Discuss the pros and cons of larger vs. smaller pull-up resistors for open-drain CMOS outputs or open-collector TTL outputs.
- 3.39 A particular LED has a voltage drop of about 2.0 V in the “on” state and requires about 5 mA of current for normal brightness. Determine an appropriate value for the pull-up resistor when the LED is connected as shown in Figure 3-52.
- 3.40 How does the answer for Drill 3.39 change if the LED is connected as shown in Figure 3-53(a)?
- 3.41 A wired-AND function is obtained simply by tying two open-drain or open-collector outputs together, without going through another level of transistor circuitry. How is it, then, that a wired-AND function can actually be slower than a discrete AND gate? (*Hint*: Recall the title of a Teenage Mutant Ninja Turtles movie.)
- 3.42 Which CMOS or TTL logic family in this chapter has the strongest output driving capability?
- 3.43 Concisely summarize the difference between HC and HCT logic families. The same concise statement should apply to AC versus ACT.
- 3.44 Why don't the specifications for FCT devices include parameters like  $V_{OLmaxC}$  that apply to CMOS loads, as HCT and ACT specifications do?
- 3.45 How do FCT-T devices reduce power consumption compared to FCT devices?
- 3.46 How many diodes are required for an  $n$ -input diode AND gate?
- 3.47 True or false: A TTL NOR gate uses diode logic.
- 3.48 Are TTL outputs more capable of sinking current or sourcing current?
- 3.49 Compute the maximum fanout for each of the following cases of a TTL output driving multiple TTL inputs. Also indicate how much “excess” driving capability is available in the LOW or HIGH state for each case.
- |                       |                        |
|-----------------------|------------------------|
| (a) 74LS driving 74LS | (b) 74LS driving 74S   |
| (c) 74S driving 74AS  | (d) 74F driving 74S    |
| (e) 74AS driving 74AS | (f) 74AS driving 74F   |
| (g) 74ALS driving 74F | (h) 74AS driving 74ALS |
- 3.50 Which resistor dissipates more power, the pull-down for an unused LS-TTL NOR-gate input, or the pull-up for an unused LS-TTL NAND-gate input? Use the maximum allowable resistor value in each case.
- 3.51 Which would you expect to be faster, a TTL AND gate or a TTL AND-OR-INVERT gate? Why?
- 3.52 Describe the key benefit and the key drawback of Schottky transistors in TTL.
- 3.53 Using the data sheet in Table 3-12, determine the worst-case LOW-state and HIGH-state DC noise margins of the 74LS00.

- 3.54 Sections 3.10.2 and 3.10.3 define eight different electrical parameters for TTL circuits. Using the data sheet in Table 3-12, determine the worst-case value of each of these for the 74LS00.
- 3.55 For each of the following resistive loads, determine whether the output drive specifications of the 74LS00 over the commercial operating range are exceeded. (Refer to Table 3-12, and use  $V_{OLmax} = 0.5\text{ V}$  and  $V_{CC} = 5.0\text{ V}$ .)
- (a)  $470\ \Omega$  to  $V_{CC}$
  - (b)  $330\ \Omega$  to  $V_{CC}$  and  $470\ \Omega$  to GND
  - (c)  $10\text{ K}\Omega$  to GND
  - (d)  $390\ \Omega$  to  $V_{CC}$  and  $390\ \Omega$  to GND
  - (e)  $600\ \Omega$  to  $V_{CC}$
  - (f)  $510\ \Omega$  to  $V_{CC}$  and  $510\ \Omega$  to GND
  - (g)  $4.7\text{ K}\Omega$  to GND
  - (h)  $220\ \Omega$  to  $V_{CC}$  and  $330\ \Omega$  to GND
- 3.56 Compute the LOW-state and HIGH-state DC noise margins for each of the following cases of a TTL output driving a TTL-compatible CMOS input, or vice versa.
- (a) 74HCT driving 74LS
  - (b) 74VHCT driving 74AS
  - (c) 74LS driving 74HCT
  - (d) 74S driving 74VHCT
- 3.57 Compute the maximum fanout for each of the following cases of a TTL-compatible CMOS output driving multiple inputs in a TTL logic family. Also indicate how much “excess” driving capability is available in the LOW or HIGH state for each case.
- (a) 74HCT driving 74LS
  - (b) 74HCT driving 74S
  - (c) 74VHCT driving 74AS
  - (d) 74VHCT driving 74LS
- 3.58 For a given load capacitance and transition rate, which logic family in this chapter has the lowest dynamic power dissipation?

### Exercises

- 3.59 Design a CMOS circuit that has the functional behavior shown in Figure X3.59. (*Hint:* Only six transistors are required.)
- 3.60 Design a CMOS circuit that has the functional behavior shown in Figure X3.60. (*Hint:* Only six transistors are required.)
- 3.61 Draw a circuit diagram, function table, and logic symbol in the style of Figure 3-19 for a CMOS gate with two inputs A and B and an output Z, where  $Z=1$  if  $A=0$  and  $B=1$ , and  $Z=0$  otherwise. (*Hint:* Only six transistors are needed.)

Figure X3.59

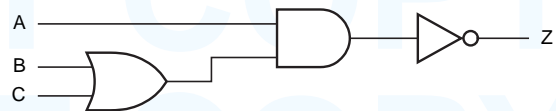
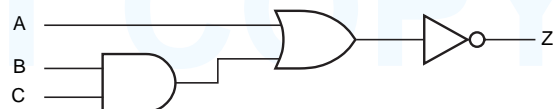


Figure X3.60



- 3.62 Draw a circuit diagram, function table, and logic symbol in the style of Figure 3-19 for a CMOS gate with two inputs A and B and an output Z, where  $Z=0$  if  $A=1$  and  $B=0$ , and  $Z=1$  otherwise. (*Hint*: Only six transistors are needed.)
- 3.63 Draw a figure showing the logical structure of an 8-input CMOS NOR gate, assuming that at most 4-input gate circuits are practical. Using your general knowledge of CMOS characteristics, select a circuit structure that minimizes the NOR gate's propagation delay for a given silicon area, and explain why this is so.
- 3.64 The circuit designers of TTL-compatible CMOS families presumably could have made the voltage drop across the "on" transistor under load in the HIGH state as little as it is in the LOW state, simply by making the  $p$ -channel transistors bigger. Why do you suppose they didn't bother to do this?
- 3.65 How much current and power are "wasted" in Figure 3-32(b)?
- 3.66 Perform a detailed calculation of  $V_{OUT}$  in Figures 3-34 and 3-33. (*Hint*: Create a Thévenin equivalent for the CMOS inverter in each figure.)
- 3.67 Consider the dynamic behavior of a CMOS output driving a given capacitive load. If the resistance of the charging path is double the resistance of the discharging path, is the rise time exactly twice the fall time? If not, what other factors affect the transition times?
- 3.68 Analyze the fall time of the CMOS inverter output of Figure 3-37, with  $R_L=1\text{ k}\Omega$  and  $V_L=2.5\text{ V}$ . Compare your result with the result in Section 3.6.1 and explain.
- 3.69 Repeat Exercise 3.68 for rise time.
- 3.70 Assuming that the transistors in an FCT CMOS three-state buffer are perfect zero-delay on-off devices that switch at an input threshold of 1.5 V, determine the value of  $t_{PLZ}$  for the test circuit and waveforms in Figure 3-24. (*Hint*: You have to determine the time using an  $RC$  time constant.) Explain the difference between your result and the specifications in Table 3-3.
- 3.71 Repeat Exercise 3.70 for  $t_{PHZ}$ .
- 3.72 Using the specifications in Table 3-7, estimate the "on" resistances of the  $p$ -channel and  $n$ -channel transistors in 74VHC-series CMOS logic.
- 3.73 Create a  $4 \times 4 \times 2 \times 2$  matrix of worst-case DC noise margins for the following CMOS interfacing situations: an (HC, HCT, VHC, or VHCT) output driving an (HC, HCT, VHC, or VHCT) input with a (CMOS, TTL) load in the (LOW, HIGH) state; Figure X3.73 illustrates. (*Hints*: There are 64 different combinations, but many give identical results. Some combinations yield negative margins.)

		Input							
		HC		HCT		VHC		VHCT	
Output	HC	CL	TL	CL	TL	CL	TL	CL	TL
	HCT	CH	TH	CH	TH	CH	TH	CH	TH
VHC	HC	CL	TL	CL	TL	CL	TL	CL	TL
	HCT	CH	TH	CH	TH	CH	TH	CH	TH
VHCT	HC	CL	TL	CL	TL	CL	TL	CL	TL
	HCT	CH	TH	CH	TH	CH	TH	CH	TH

Key:  
 CL = CMOS load, LOW  
 CH = CMOS load, HIGH  
 TL = TTL load, LOW  
 TH = TTL load, HIGH

Figure X3.73

- 3.74 Using Figure 3-85, determine the DC noise margins for 5-V-tolerant, 3.3-V CMOS driving 5-V CMOS logic with TTL input levels, and vice versa.
- 3.75 Using Figure 3-85, determine the DC noise margins for 3.3-V-tolerant, 2.5-V CMOS driving 3.3-V CMOS, and vice versa.
- 3.76 In the LED example in Section 3.7.5, a designer chose a resistor value of 300  $\Omega$  and found that the open-drain gate was able to maintain its output at 0.1 V while driving the LED. How much current flows through the LED, and how much power is dissipated by the pull-up resistor in this case?
- 3.77 Consider a CMOS 8-bit binary counter (Section 8.4) clocked at 16 MHz. For the purpose of computing the counter's dynamic power dissipation, what is the transition frequency of the least significant bit? Of the most significant bit? For the purpose of determining the dynamic power dissipation of the eight output bits, what frequency should be used?
- 3.78 Using only AND and NOR gates, draw a logic diagram for the logic function performed by the circuit in Figure 3-55.
- 3.79 Calculate the approximate output voltage at Z in Figure 3-56, assuming that the gates are HCT-series CMOS.
- 3.80 Redraw the circuit diagram of a CMOS 3-state buffer in Figure 3-48 using actual transistors instead of NAND, NOR, and inverter symbols. Can you find a circuit for the same function that requires a smaller total number of transistors? If so, draw it.
- 3.81 Modify the CMOS 3-state buffer circuit in Figure 3-48 so that the output is in the High-Z state when the enable input is HIGH. The modified circuit should require no more transistors than the original.
- 3.82 Using information in Table 3-3, estimate how much current can flow through each output pin if the outputs of two different 74HC00s are fighting.
- 3.83 Show that at a given power-supply voltage, an FCT-type  $I_{CCD}$  specification can be derived from an HCT/ACT-type  $C_{PD}$  specification, and vice versa.
- 3.84 If both  $V_Z$  and  $V_B$  in Figure 3-65(b) are 4.6 V, can we get  $V_C = 5.2$  V? Explain.
- 3.85 Modify the program in Table 3-10 to account for leakage current in the OFF state.
- 3.86 Assuming "ideal" conditions, what is the minimum voltage that will be recognized as a HIGH in the TTL NAND gate in Figure 3-75 with one input LOW and the other HIGH?
- 3.87 Assuming "ideal" conditions, what is the maximum voltage that will be recognized as a LOW in the TTL NAND gate in Figure 3-75 with both inputs HIGH?
- 3.88 Find a commercial TTL part that can source 40 mA in the HIGH state. What is its application?
- 3.89 What happens if you try to drive an LED with its cathode grounded and its anode connected to a TTL totem-pole output, analogous to Figure 3-53(b) for CMOS?
- 3.90 What happens if you try to drive a 12-volt relay with a TTL totem-pole output?
- 3.91 Suppose that a single pull-up resistor to +5 V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much HIGH-state DC noise margin are you providing in this case?

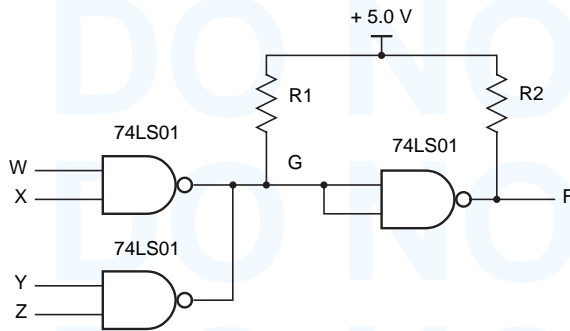


Figure X3.92

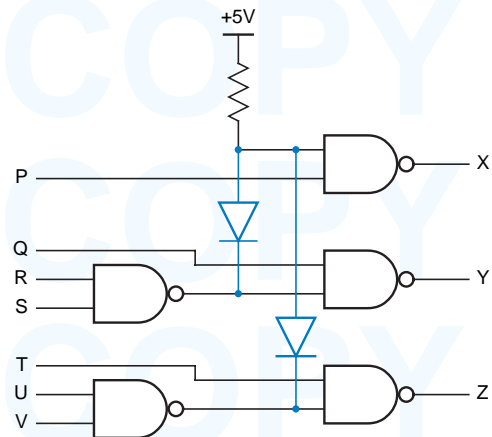


Figure X3.95

- 3.92 The circuit in Figure X3.92 uses open-collector NAND gates to perform “wired logic.” Write a truth table for output signal F and, if you’ve read Section 4.2, a logic expression for F as a function of the circuit inputs.
- 3.93 What is the maximum allowable value for  $R1$  in Figure X3.92? Assume that a 0.7-V HIGH-state noise margin is required. The 74LS01 has the specs shown in the 74LS column of Table 3-11, except that  $I_{OHmax}$  is  $100\ \mu A$ , a leakage current that flows *into* the output in the HIGH state.
- 3.94 Suppose that the output signal F in Figure X3.92 drives the inputs of two 74S04 inverters. Compute the minimum and maximum allowable values of  $R2$ , assuming that a 0.7 V HIGH-state noise margin is required.
- 3.95 A logic designer found a problem in a certain circuit’s function after the circuit had been released to production and 1000 copies of it built. A portion of the circuit is shown in Figure X3.95 in black; all of the gates are 74LS00 NAND gates. The logic designer fixed the problem by adding the two diodes shown in color. What do the diodes do? Describe both the logical effects of this change on the circuit’s function and the electrical effects on the circuit’s noise margins.
- 3.96 A 74LS125 is a buffer with a three-state output. When enabled, the output can sink 24 mA in the LOW state and source 2.6 mA in the HIGH state. When disabled, the output has a leakage current of  $\pm 20\ \mu A$  (the sign depends on the output voltage—plus if the output is pulled HIGH by other devices, minus if it’s LOW). Suppose a system is designed with multiple modules connected to a bus, where each module has a single 74LS125 to drive the bus and one 74LS04 to receive information on the bus. What is the maximum number of modules that can be connected to the bus without exceeding the 74LS125’s specs?
- 3.97 Repeat Exercise 3.97, this time assuming that a single pull-up resistor is connected from the bus to +5 V to guarantee that the bus is HIGH when no device is driving it. Calculate the maximum possible value of the pull-up resistor, and the number of modules that can be connected to the bus.
- 3.98 Find the circuit design in a TTL data book for an actual three-state gate, and explain how it works.

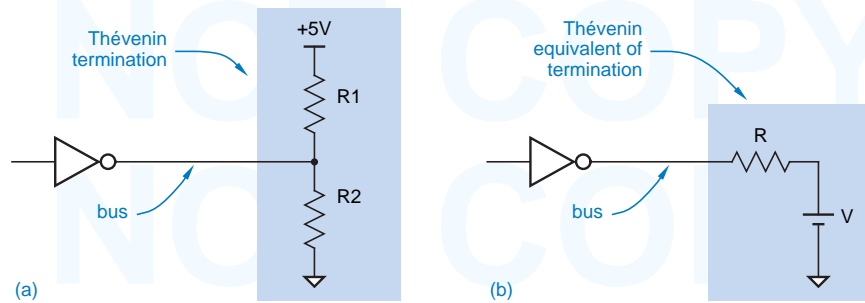


Figure X3.99

3.99 A *Thévenin termination* for an open-collector or three-state bus has the structure shown in Figure X3.99(a). The idea is that, by selecting appropriate values of  $R1$  and  $R2$ , a designer can obtain a circuit equivalent to the termination in (b) for any desired values of  $V$  and  $R$ . The value of  $V$  determines the voltage on the bus when no device is driving it, and the value of  $R$  is selected to match the characteristic impedance of the bus for transmission-line purposes (Section 11.4). For each of the following pairs of  $V$  and  $R$ , determine the required values of  $R1$  and  $R2$ .

- (a)  $V = 2.75, R = 148.5$       (b)  $V = 2.7, R = 180$
- (c)  $V = 3.0, R = 130$         (d)  $V = 2.5, R = 75$

3.100 For each of the  $R1$  and  $R2$  pairs in Exercise 3.99, determine whether the termination can be properly driven by a three-state output in each of the following logic families: 74LS, 74S, 74FCT-T. For proper operation, the family's  $I_{OL}$  and  $I_{OH}$  specs must not be exceeded when  $V_{OL} = V_{OLmax}$  and  $V_{OH} = V_{OHmin}$ , respectively.

3.101 Using the graphs in a TTL data book, develop some rules of thumb for derating the maximum-propagation-delay specification of LS-TTL under nonoptimal conditions of power-supply voltage, temperature, and loading.

3.102 Determine the total power dissipation of the circuit in Figure X3.102 as function of transition frequency  $f$  for two realizations: (a) using 74LS gates; (b) using 74HC gates. Assume that input capacitance is 3 pF for a TTL gate and 7 pF for a CMOS gate, that a 74LS gate has an internal power-dissipation capacitance of 20 pF, and that there is an additional 20 pF of stray wiring capacitance in the circuit. Also assume that the X, Y, and Z inputs are always HIGH, and that input C is driven with a CMOS-level square wave with frequency  $f$ . Other information that you need for this problem can be found in Tables 3-5 and 3-11. State any other assumptions that you make. At what frequency does the TTL circuit dissipate less power than the CMOS circuit?

Figure X3.102

