3e3.1

3.201 A particular logic family defines a LOW signal to be in the range 0.0–0.8 V and a HIGH signal to be in the range 2.0–3.3 V. Under a positive-logic convention, indicate the logic value associated with each of the following signal levels:

(a) 0.0 V (b) 3.0 V (c) 0.8 V (d) 1.9 V

(e) 2.0 V (f) 5.0 V (g) –0.7 V (h) –3.0 V

3e3.2 3.202 Repeat Drill 3.1 using a negative-logic convention.

3e3.5

3.203 True or false: For a given set of input values, a NAND gate produces the opposite output as a NOR gate.

3e3.7 3.204 What kind of transistors are used in CMOS gates?

3e3.8 3.205 (Hobbyists only.) Draw an equivalent circuit for a CMOS inverter using a single-pole, double-throw relay.

3e3.15

3.206 Name and draw the logic symbols of four different 4-input CMOS gates that each use 8 transistors.

3e3.19

3.207 How much high-state DC noise margin is available in a CMOS inverter whose transfer characteristic under worst-case conditions looks like Figure 3-25? How much low-state DC noise margin is available? (Assume standard 1.5-V and 3.5-V thresholds for LOW and HIGH.)

3e3.22 3.208 Based on the conventions and definitions in Section 3.4, if the current at a device output is specified as a negative number, is the output sourcing current or sinking current?

3e3.23

3.209 For each of the following resistive loads, determine whether the output drive specifications of the 74HC00 over the commercial operating range are exceeded. (Refer to Table 3-3, and use V_{OHmin} = 3.84 V and V_{CC} = 5.0 V.)

(a) 120 Ω to V_{CC}

(b) 270 Ω to V_{CC} and 330 Ω to GND

(c) 1 kΩ to GND

(d) 150 Ω to V_{CC} and 150 Ω to GND

(e) 100 Ω to V_{CC}

(f) 75 Ω to V_{CC} and 150 Ω to GND

(g) 75 Ω to V_{CC}

(h) 270 Ω to V_{CC} and 150 Ω to GND

3e3.25 3.210 Determine the LOW-state and HIGH-state DC fanout of the 74HC00 when it drives 74LS00-like inputs. (Refer to Tables 3-3 and 3-11.)

3e3.29 3.211 Explain why putting all the decoupling capacitors in one corner of a printed-circuit board is not a good idea.

3e3.31 3.212 Name the two components of CMOS logic gate's delay. Which one is most affected by load capacitance?

3e3.32

3.213 Determine the *RC* time constant for each of the following resistor-capacitor combinations:

(a) $R = 100\ \Omega$, $C = 50$ pF (b) $R = 330\ \Omega$, $C = 150$ pF

(c) $R = 1$ kΩ, $C = 30$ pF (d) $R = 4.7$ kΩ, $C = 100$ pF

3e3.33 3.214 Besides delay, what other characteristic(s) of a CMOS circuit are affected by load capacitance?

3e3.35 3.215 It is possible to operate 74VHC CMOS devices with a 3.3-volt power supply. How much power does this typically save, compared to 5-volt operation?

3e3.36 3.216 A particular Schmitt-trigger inverter has V_{ILmax} = 0.8 V, V_{IHmin} = 2.0 V, V_{T+} = 1.6 V, and V_{T-} = 1.3 V. How much hysteresis does it have?

3e3.37 3.217 Why are three-state outputs usually designed to turn off faster than they turn on?

3e3.39 3.218 A particular LED has a voltage drop of about 2.0 V in the "on" state and requires about 5 mA of current for normal brightness. Determine an appropriate value for the pull-up resistor when the LED is connected as shown in Figure 3-53.

3e3.40 3.219 How does the answer for Drill 3.39 change if the LED is connected as shown in Figure 3-54(a)?

3e3.43 3.220 Concisely summarize the difference between HC and HCT logic families. The same concise statement should apply to AC versus ACT.

3e3.47 3.221 True or false: A TTL NOR gate uses diode logic.

3e3.49

3.222 Compute the maximum fanout for each of the following cases of a TTL output driving multiple TTL inputs. Also indicate how much "excess" driving capability is available in the LOW or HIGH state for each case.

(a) 74LS driving 74LS
(b) 74LS driving 74S
(c) 74S driving 74AS
(d) 74F driving 74S
(e) 74AS driving 74AS
(f) 74AS driving 74F
(g) 74ALS driving 74F
(h) 74AS driving 74ALS

3e3.51 3.223 Which would you expect to be faster, a TTL AND gate or a TTL AND-OR-INVERT gate? Why?

3e3.53 3.224 Using the data sheet in Table 3-11, determine the worst-case LOW-state and HIGH-state DC noise margins of the 74LS00.

3e3.54

3.225 Sections 3.10.4 and 3.10.5 define eight different electrical parameters for TTL circuits. Using the data sheet in Table 3-11, determine the worst-case value of each of these for the 74LS00.

3e3.55

3.226 For each of the following resistive loads, determine whether the output drive specifications of the 74LS00 over the commercial operating range are exceeded. (Refer to Table 3-11, and use $V_{OLmax} = 0.5$ V and $V_{CC} = 5.0$ V.)

(a) 470 Ω to V_{CC}
(b) 330 Ω to V_{CC} and 470 Ω to GND
(c) 10 kΩ to GND
(d) 390 Ω to V_{CC} and 390 Ω to GND
(e) 600 Ω to V_{CC}
(f) 510 Ω to V_{CC} and 510 Ω to GND
(g) 4.7 kΩ to GND
(h) 220 Ω to V_{CC} and 330 Ω to GND

3e3.56

3.227 Compute the LOW-state and HIGH-state DC noise margins for each of the following cases of a TTL output driving a TTL-compatible CMOS input, or vice versa.

(a) 74HCT driving 74LS (b) 74VHCT driving 74AS

(c) 74LS driving 74HCT (d) 74S driving 74VHCT

3e3.57

3.228 Compute the maximum fanout for each of the following cases of a TTL-compatible CMOS output driving multiple inputs in a TTL logic family. Also indicate how much "excess" driving capability is available in the LOW or HIGH state for each case.

(a) 74HCT driving 74LS (b) 74HCT driving 74S

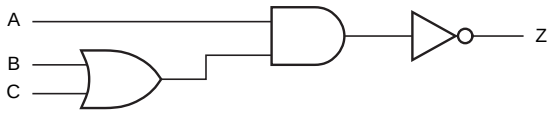
(c) 74VHCT driving 74AS (d) 74VHCT driving 74LS

3e3.58 3.229 For a given load capacitance and transition rate, which logic family in this chapter has the lowest dynamic power dissipation?

3e3.59

3.230 Design a CMOS circuit that has the functional behavior shown in Figure X3.230. (*Hint:* Only six transistors are required.)

Figure X3.230



3e3.60

3.231 Design a CMOS circuit that has the functional behavior shown in Figure X3.231. (*Hint:* Only six transistors are required.)

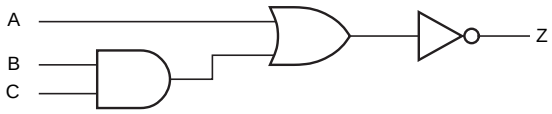


Figure X3.231

3e3.63 3.232 Draw a figure showing the logical structure of an 8-input CMOS NOR gate, assuming that at most 4-input gate circuits are practical. Using your general knowledge of CMOS characteristics, select a circuit structure that minimizes the NOR gate's propagation delay for a given silicon area, and explain why this is so.

3e3.68

3.233 Analyze the fall time of the CMOS inverter output of Figure 3-37, with R_L=1 kΩ and V_L=2.5 V. Compare your result with the result in Section 3.6.1 and explain.

3e3.72 3.234 Using the specifications in Table 3-7, estimate the "on" resistances of the *p*-channel and *n*-channel transistors in 74VHC-series CMOS logic.

3e3.76

3.235 In the LED example in Section 3.7.5, a designer chose a resistor value of 300 Ω and found that the open-drain gate was able to maintain its output at 0.1 V while driving the LED. How much current flows through the LED, and how much power is dissipated by the pull-up resistor in this case?

3e3.85 3.236 Modify the program in Table BJT-1 to account for leakage current in the OFF state.

3e3.91 3.237 Suppose that a single pull-up resistor to +5 V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much HIGH-state DC noise margin are you providing in this case?

3e3.93

3.238 What is the maximum allowable value for *R1* in Figure xTTL.10? Assume that a 0.7-V HIGH-state noise margin is required. The 74LS01 has the specs shown in the 74LS column of Table 3-10, except that I_{OHmax} is 100 μA, a leakage current that flows *into* the output in the HIGH state.

3e3.94 3.239 Suppose that the output signal F in Figure xTTL.10 drives the inputs of two 74S04 inverters. Compute the minimum and maximum allowable values of *R2*, assuming that a 0.7 V HIGH-state noise margin is required.

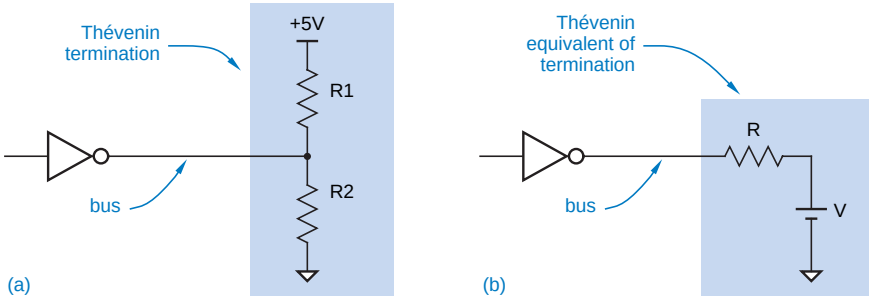
3e3.99

3.240 A *Thévenin termination* for an open-collector or three-state bus has the structure shown in Figure X3.87(a). The idea is that, by selecting appropriate values of *R1* and *R2*, a designer can obtain a circuit equivalent to the termination in (b) for any desired values of *V* and *R*. The value of *V* determines the voltage on the bus when no device is driving it, and the value of *R* is selected to match the characteristic impedance of the bus for transmission-line purposes (Section 11.4). For each of the following pairs of *V* and *R*, determine the required values of *R1* and *R2*.

(a) $V = 2.75$, $R = 148.5$ (b) $V = 2.7$, $R = 180$

(c) $V = 3.0$, $R = 130$ (d) $V = 2.5$, $R = 75$

Figure X3.240



3e3.100 3.241 For each of the *R1* and *R2* pairs in Exercise 3.87, determine whether the termination can be properly driven by a three-state output in each of the following logic families: 74LS, 74S, 74FCT-T. For proper operation, the family's I_{OL} and I_{OH} specs must not be exceeded when $V_{OL} = V_{OLmax}$ and $V_{OH} = V_{OHmin}$, respectively.