3e5.1

6.201 Give three examples of combinational logic circuits that require *billions and billions* of rows to describe in a truth table. For each circuit, describe its inputs and output(s) and indicate exactly how many rows the truth table contains; you need not write out the truth table. (*Hint:* You can find several such circuits in Chapter 6.)

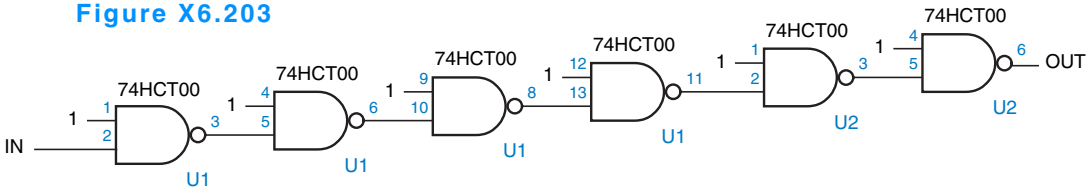
3e5.6

6.202 True or false: In bubble-to-bubble logic design, outputs with a bubble can be connected only to inputs with a bubble.

3e5.9

6.203 Determine the exact maximum propagation delay from IN to OUT of the circuit in Figure X6.203 for both LOW-to-HIGH and HIGH-to-LOW transitions, using the timing information given in Table 6-2. Repeat, using a single worst-case delay number for each gate, and compare and comment on your results.

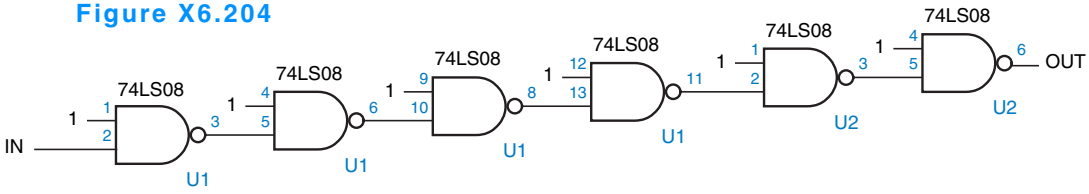
Figure X6.203



3e5.10

6.204 Determine the exact maximum propagation delay from IN to OUT of the circuit in Figure X6.204 for both LOW-to-HIGH and HIGH-to-LOW transitions, using the timing information given in Table 6-2. Repeat, using a single worst-case delay number for each gate, and compare and comment on your results.

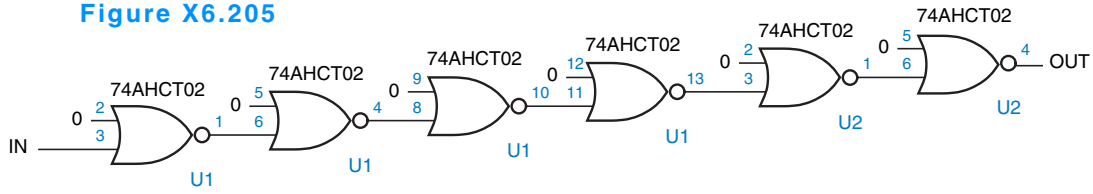
Figure X6.204



3e5.11

6.205 Determine the typical propagation delay from IN to OUT of the circuit in Figure X6.205 for both LOW-to-HIGH and HIGH-to-LOW transitions, using the timing information given in Table 6-2. Repeat, using a single worst-case delay number for each gate, and compare and comment on your results.

Figure X6.205



3e5.17

6.206 Using the information in Table 6-3 for 74AHCT components, determine the maximum propagation delay from any input to any output in the 5-to-32 decoder circuit of Figure 6-37. You may use the "worst-case" analysis method.

3e5.19

6.207 Show how to build each of the following single- or multiple-output logic functions using one or more 74x138 or 74x139 binary decoders and NAND gates. (*Hint:* Each realization should be equivalent to a sum of minterms.)

(a) $F = \Sigma_{X,Y,Z}(2,4,7)$

(b) $F = \prod_{A,B,C}(3,4,5,6,7)$

(c) $F = \Sigma_{A,B,C,D}(2,4,6,14)$

(d) $F = \Sigma_{W,X,Y,Z}(0,1,2,3,5,7,11,13)$

(e) $F = \Sigma_{W,X,Y}(1,3,5,6)$
$G = \Sigma_{W,X,Y}(2,3,4,7)$

(f) $F = \Sigma_{A,B,C}(0,4,6)$
$G = \Sigma_{C,D,E}(1,2)$

3e5.23

6.208 Using the information in Tables 6-2 and 6-3 for 74HCT components, determine the maximum propagation delay from any input to any output in the 32-to-1 multiplexer circuit of Figure 6-62. You may use the "worst-case" analysis method.

3e5.24

6.209 An n-input parity tree can be built with XOR gates in the style of Figure 6-70(a). Under what circumstances does a similar n-input parity tree built using XNOR gates perform exactly the same function?

3e5.26

6.210 Using the information in Tables 6-2 and 6-3 for 74HCT components, determine the maximum propagation delay from the DU bus to the DC bus in the error-correction circuit of Figure 6-73. You may use the "worst-case" analysis method.

3e5.27

6.211 Starting with the equations given in Section 6.9.4, write a complete logic expression for the ALTBOUT output of the 74x85.

3e5.28

6.212 Write an algebraic expression for s_2, the third sum bit of a binary adder, as a function of inputs x_0, x_1, x_2, y_0, y_1, and y_2. Assume that $c_0 = 0$, and do not attempt to "multiply out" or minimize the expression.

3e5.29 6.213 Starting with the logic diagram for the 74x682, write a logic expression for the PGTQ_L output in terms of the inputs.

G5.231 6.214 A possible definition of a BUT gate, as in Exercise 6.31, is "Y1 is 1 if A1 and B1 are 1 *but* either A2 or B2 is 0; Y2 is defined symmetrically." Write the truth table and find minimal product-of-sums expressions for the BUT-gate outputs. Draw the logic diagram for a NOR-NOR circuit for the expressions, assuming that only uncomplemented inputs are available. You may use multiple-input NOR gates and inverters.

3e5.32

6.215 A possible definition of a BUT gate, as in Exercise 6.31, is "Y1 is 1 if A1 and B1 are 1 *but* either A2 or B2 is 0; Y2 is defined symmetrically."Find a gate-level design such a BUT gate that uses a minimum number of transistors when realized in CMOS. You may use gates from 74x00, '02, '04, '10, '20, and '30 packages. Write the output expressions (which need not be two-level sums of products), and draw the logic diagram.

3e5.33

6.216 For each circuit in Exercises 6.214 and 6.215, compute the worst-case delay from input to output, using the delay numbers for 74HCT components in Table 6-2. Compare the cost (number of transistors), speed, and input loading of the two designs. Which is better?

3e5.34

6.217 A possible definition of a BUT gate, as in Exercise 6.31, is "Y1 is 1 if A1 and B1 are 1 *but* either A2 or B2 is 0; Y2 is defined symmetrically. Butify the function $F = \Sigma_{W,X,Y,Z}(3,7,11,12,13,14)$. That is, show how to perform F with a single BUT gate as defined in Exercise 6.31 and a single 2-input OR gate.

3e5.35

6.218 Suppose that a 74LS138 decoder is connected so that all enable inputs are asserted and C B A = 101. Using the information in Table 6-3 and the '138 internal logic diagram, determine the propagation delay from input to all relevant outputs for each possible single-input change. (*Hint:* There are a total of nine delay numbers, since a change on A, B, or C affects two outputs, and a change on any of the three enable inputs affects one output.)

3e5.85

6.219 Design a customized decoder with the function table in Table X6.219 using MSI and SSI parts. Minimize the number of IC packages in your design.

Table X6.219

CS_L	A2	A1	A0	***Output to Assert***
1	x	x	x	none
0	0	0	x	BILL_L
0	0	x	0	MARY_L
0	0	1	x	JOAN_L
0	0	x	1	PAUL_L
0	1	0	x	ANNA_L
0	1	x	0	FRED_L
0	1	1	x	DAVE_L
0	1	x	1	KATE_L

3e5.42

6.220 Twenty years ago, a famous logic designer decided to quit teaching and make a fortune by licensing the circuit design shown in Figure X6.220.

(a) Label the inputs and outputs of the circuit with appropriate signal names, including active-level indications.

(b) What does the circuit do? Be specific and account for all inputs and outputs.

(c) Draw the logic symbol that would go on the data sheet of this circuit.

(d) Write an ABEL or behavioral VHDL or Verilog program for the circuit.

(e) With what standard building blocks did the new circuit compete? Do you think it was successful as an MSI part?

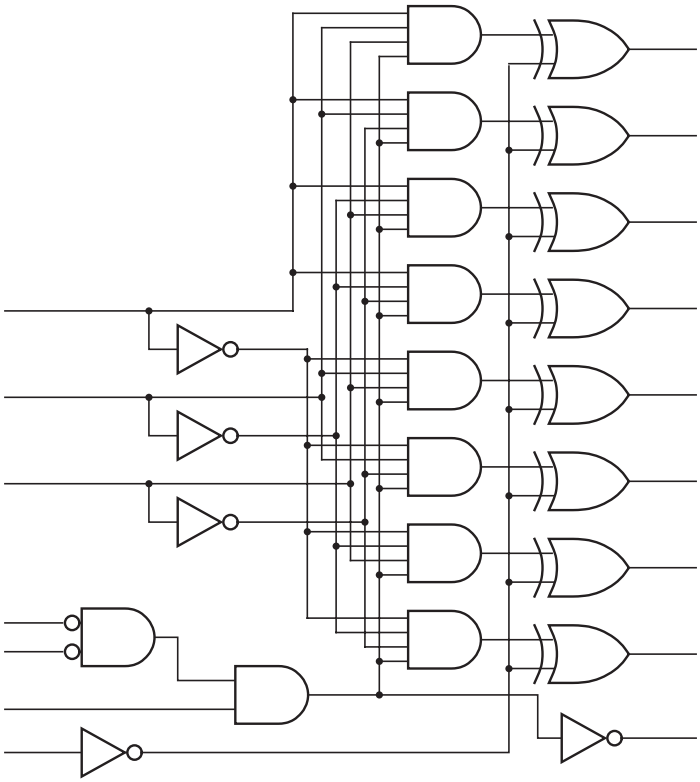


Figure X6.220

3e5.43

6.221 An FCT three-state buffer drives ten FCT inputs and a 4.7-KΩ pull-up resistor to 5.0 V. When the output changes from LOW to Hi-Z, estimate how long it takes for the FCT inputs to see the output as HIGH. State any assumptions that you make.

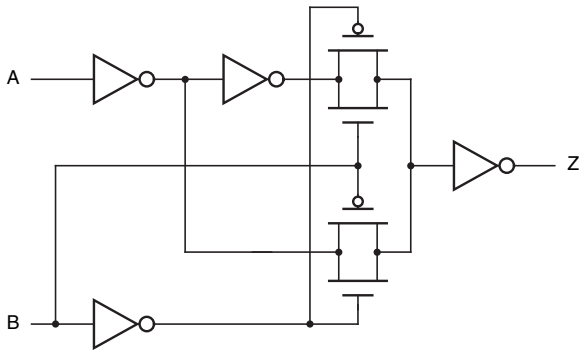
3e5.44

6.222 On a three-state bus, ten FCT three-state buffers are driving ten FCT inputs and a 4.7-KΩ pull-up resistor to 5.0 V. Assuming that no other devices are driving the bus, estimate how long the bus signal remains at a valid logic level when an active output enters the Hi-Z state. State any assumptions that you make.

3e5.45 6.223 Design a 10-to-4 encoder with inputs in the 1-out-of-10 code and outputs in BCD.

3e5.56 6.224 What logic function is performed by the CMOS circuit shown in Figure X6.224?

Figure X6.224



3e5.61

6.225 Show how to realize the 4-input, 18-bit multiplexer with the functionality of Table 6-46 using 9 74x153s and a "code converter" with inputs S2–S0 and outputs C1, C0 such that [C1, C0] = 00–11 when S2–S0 selects A–D, respectively.

3e5.62

6.226 Design a 3-input, 2-output combinational circuit that performs the code conversion specified in Exercise 6.225, using discrete gates.

3e5.71 6.227 Design a 16-bit comparator using five 74x85s in a treelike structure, such that the maximum delay for a comparison equals twice the delay of one 74x85.

3e5.77

6.228 Starting with the logic diagram for the 74x283 in Figure 6-87, write a logic expression for the S2 output in terms of the inputs, and prove that it does indeed equal the third sum bit in a binary addition as advertised. You may assume that $c_0 = 0$ (i.e., ignore c_0).

6.229 Write a structural VHDL or Verilog program for an 8-bit carry-lookahead adder, similar in structure to the 74x283 4-bit adder. Use the language's "`generate`" capability.

3e5.78

6.230 Referring to the data sheet of a 74S182 carry lookahead circuit, determine whether or not its outputs match the equations given in Section 6.10.7.

3e5.80

6.231 Draw the logic diagram for a 64-bit ALU using sixteen 74x181s and five 74S182s for full carry lookahead (two levels of '182s). For the '181s, you need show only the CIN inputs and G_L and P_L outputs.