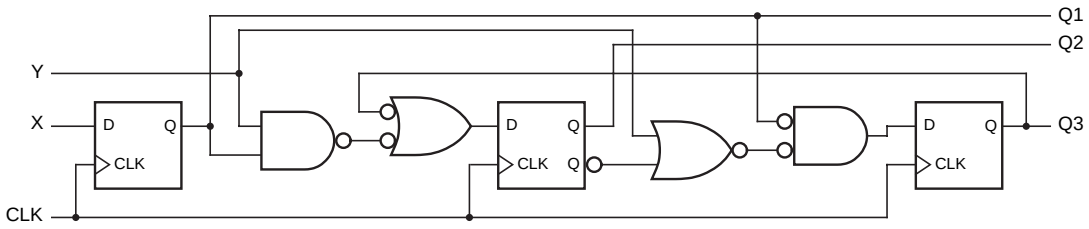
7.201 Give three examples of metastability that occur in everyday life, other than ones discussed in this chapter. 3e7.1

7.202 Show how to build a flip-flop equivalent to the 74x109 positive-edge-triggered J-$\overline{K}$ flip-flop using a 74x74 positive-edge-triggered D flip-flop and one or more gates from a 74x00 package. 3e7.7

7.203 Repeat Drill 7.12, swapping AND and OR gates in the logic diagram. Is the new state/output table the "dual" of the original one? Explain. 3e7.10

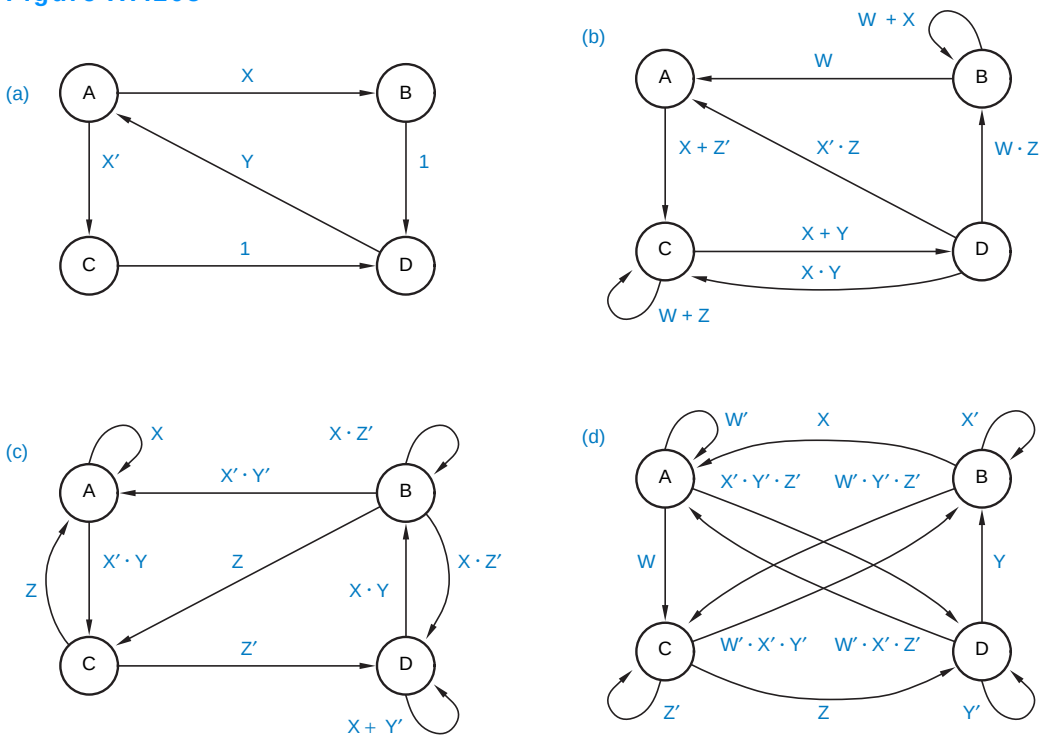
7.204 Analyze the clocked synchronous state machine in Figure X7.204. Write excitation equations, excitation/transition table, and state/output table (use state names A–H for Q1 Q2 Q3 = 000–111). 3e7.16

Figure X7.204



7.205 All of the state diagrams in Figure X7.205 are ambiguous. List all of the ambiguities in these state diagrams. (*Hint:* Use Karnaugh maps where necessary to find uncovered and double-covered input combinations.) 3e7.20

Figure X7.205



7.206 Modify the state diagram of Figure 7-58 so that the machine goes into hazard mode immediately if LEFT and RIGHT are asserted simultaneously during a turn. Write the corresponding transition list. 3e7.23

7.207 Using ABEL and a GAL16V8 PLD, design a clocked synchronous state machine that checks a serial data line for even parity. The circuit should have two inputs, SYNC and DATA, in addition to CLOCK, and one Moore-type output, ERROR. You should be able to do the job using just four states. Your program should use an ABEL `state_diagram`. It should define the state assignments and include comments that describe each state's meaning. 3e7.33

7.208 Write a new transition table and derive minimal-cost excitation and output equations for the state table in Table 7-5 using the "simplest" state assignment in Table 7-6 and D flip-flops. Compare the cost of your excitation and output equations with the ones derived on page 565. 3e7.36

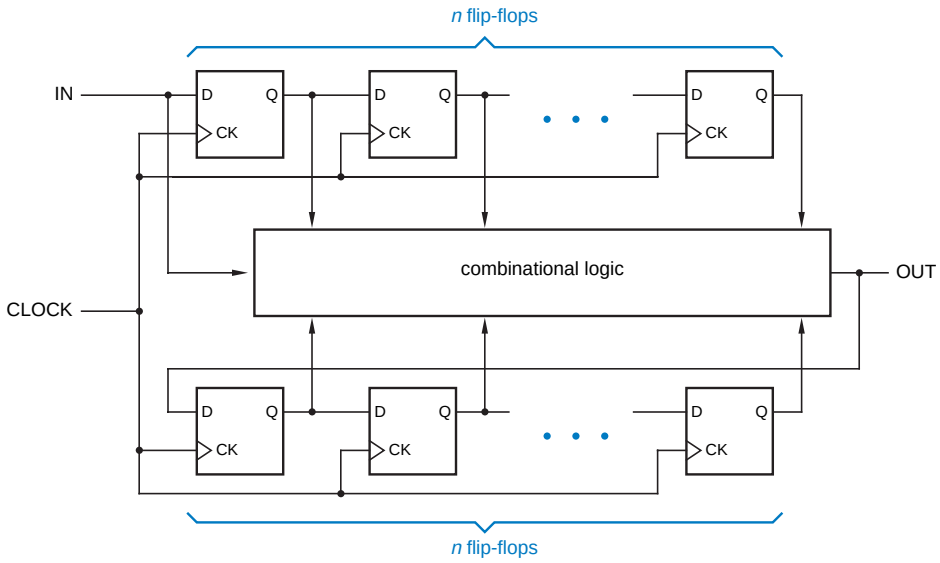
7.209 Suppose that the state machine with the equations derived on page 565 is to be built using 74LS74 D flip-flops. What signals should be applied to the flip-flop preset and clear inputs? 3e7.38

finite-memory machine

3e7.56

7.210 The output of a *finite-memory machine* is completely determined by its current input and its inputs and outputs during the previous n clock ticks, where n is a finite, bounded integer. For example, Figure X7.210 shows the realization of a finite-memory machine with one input and one output. Note that a finite-*state* machine need not be a finite-*memory* machine; for example, a modulo-n counter with an enable input and a "MAX" output has only n states, but its output may depend on the value of the enable input at every clock tick since initialization. Show how to realize the combination-lock machine of Table 7-11 as a finite-memory machine.

Figure X7.210



BUT flop

7.211 A *BUT flop* may be constructed from an NBUT gate as shown in Figure X7.211 (An *NBUT gate* is simply a BUT gate with inverted outputs; see Exercise 6.31 for the definition of a BUT gate.) Analyze the BUT flop as a feedback sequential circuit and obtain excitation equations, transition table, and flow table. Is this circuit good for anything, or is it a flop?

3e7.69

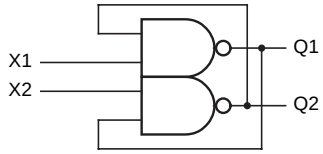


Figure X7.211

7.212 A clever student designed the circuit in Figure X7.79 to create a BUT gate. But the circuit didn't always work correctly. Analyze the circuit and explain why. 3e7.70

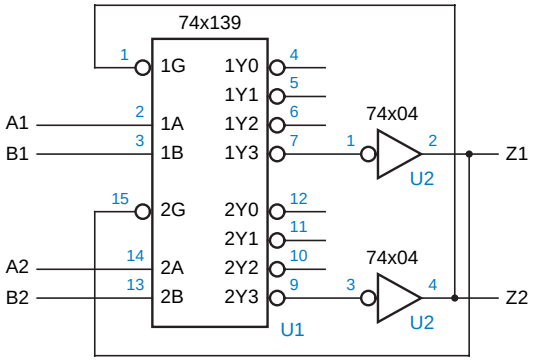


Figure X7.212