3e8.8

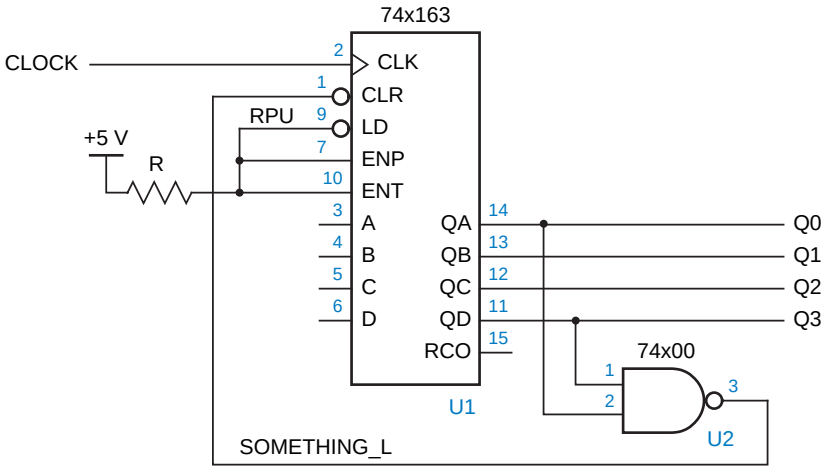
8.201 Write an ABEL program for a GAL16V8, GAL20V8, or GAL22V10 that gives it exactly the same functionality as a 74x175. Use the simplest possible device.

3e8.12

8.202 Modify the ABEL program in Table 8-14 to perform the function of a 74X169 up/down counter. Does it still fit in a 16V8?

3e8.15

8.203 What is the counting sequence of the counter circuit below? Is there a simpler circuit with the same behavior?



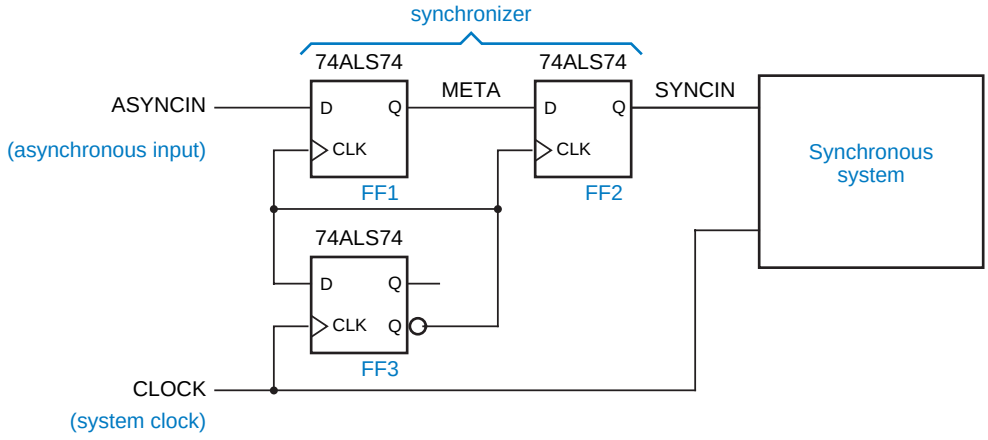
3e8.16

8.204 A 74x163 counter is hooked up with inputs ENP, ENT, A, and D always HIGH, inputs B and C always LOW, input LD_L = (QB · QC)′, and input CLR_L = (QC · QD)′. The CLK input is hooked up to a free-running clock signal. Draw a logic diagram for this circuit. Assuming that the counter starts in state 0000, write the output sequence on QD QC QB QA for the next 15 clock ticks.

3e8.18 8.205 Starting with state 0001, write the sequence of states for a 4-bit LFSR counter designed according to Figure 8-51 and Table 8-26.

3e8.21

8.206 Calculate the MTBF of the synchronizer below, assuming a clock frequency of 25 MHz and an asynchronous transition rate of 1 MHz. Assume that the setup time t_{setup} and the propagation delay t_{pd} from clock to Q or QN in a 74ALS74 are both 10 ns.



3e8.27 8.207 Design a 4-bit ripple counter using four D flip-flops and no other components.

3e8.28

8.208 What is the maximum propagation delay from clock to output for the 4-bit ripple counter of Exercise 8.207 using 74HCT flip-flops? Repeat, using 74AHCT and 74LS74 flip-flops.

3e8.36 8.209 Using a 74x163 4-bit binary counter, design a modulo-11 counter circuit with the counting sequence 3, 4, 5, …, 12, 13, 3, 4, ….

3e8.39 8.210 Design a modulo-129 counter using two 74x163s and a single inverter.

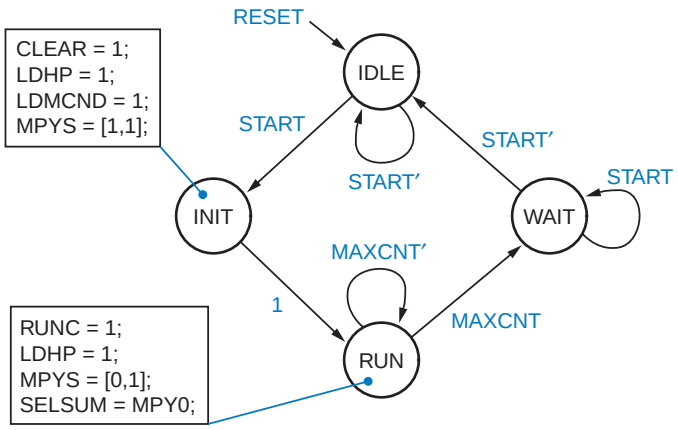
3e8.45

8.211 A digital designer (the author!) was asked at the last minute to add new functionality to a PCB that had room for just one more 16-pin MSI IC. The PCB already had a 16-MHz clock signal, MCLK, and a spare microprocessor-controlled select signal, SEL. The designer was asked to provide a new clock signal, UCLK, whose frequency would be 8 MHz or 4 MHz depending on the value of SEL. To make things worse, the PCB had no spare SSI gates, and UCLK was required to have a 50% duty cycle at both frequencies. It took the designer about five minutes to come up with a circuit. Now it's your turn to do the same. (*Hint:* The designer had long considered the 74x163 to be the fundamental building block of tricky sequential-circuit design.)

3e8.65 8.212 Find a feedback equation for a 3-bit LFSR counter, other than the one given in Table 8-26, that produces a maximum-length sequence.

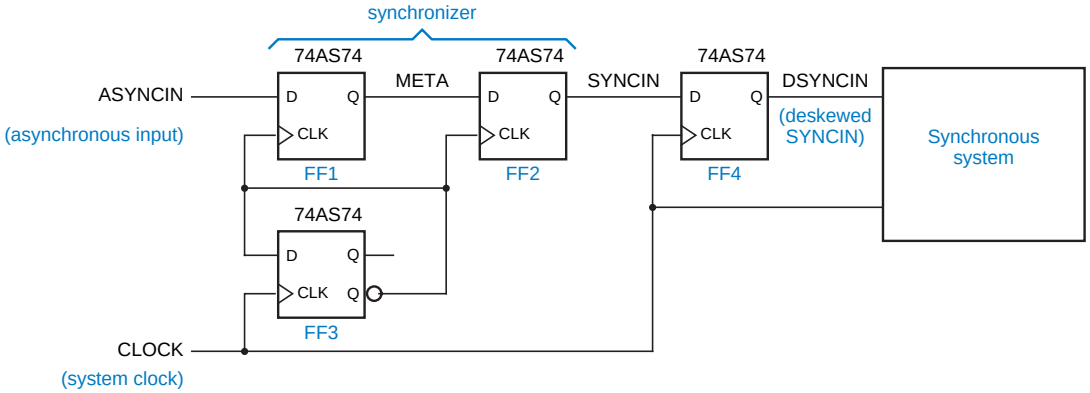
3e8.82

8.213 Write an ABEL program corresponding to the state diagram below. This state diagram is used in the control unit for the multiplier circuit in Section XSbb.3 at DDPPonline..



3e8.85 8.214 Write a VHDL program that combines the programs in the two preceding exercises to form a complete 8-bit shift-and-add multiplier.

3e8.91 8.215 The circuit in Figure X8.83 includes a deskewing flip-flop so that the synchronized output from the multiple-cycle synchronizer is available as soon as possible after the edge of CLOCK. Ignoring metastability considerations, what is the maximum frequency of CLOCK? Assume that for a 74F74, $t_{setup} = 5$ ns and $t_{pd} = 7$ ns.



3e8.94

8.216 Look up U.S. patent number 4,999,528, "Metastable-proof flip-flop," and describe why it doesn't always work as advertised. (*Hints:* Patents can be found at `www.patents.ibm.com`. There's enough information in this patent's abstract to figure out how the circuit can fail.)