3e8.19 XSbb.9The delay calculation is different, depending on the starting state.

In the INIT state, U7 and U8 take 21 ns to propagate the CLEAR signal to the outputs. Then U6 requires 20 ns setup time on its D inputs while U3 requires 20 ns setup time on its RIN input. This implies a minimum clock period of 41 ns, assuming zero delay from the control unit.

In states M1–M8, the minimum clock period depends on the delay of the combinational logic in the control unit that asserts SELSUM when MPY0 is asserted. However, the most obvious way to do this is to connect MPY0 directly to SELSUM, creating a delay of 0 ns. This assumption is made below. Also, it is assumed that MPY0 is 1 to find the worst case. The figure on the next page shows the worst-case path, in heavy lines, to be 106 ns. Since we would like to use the same clock for all states, the minimum clock period is 106 ns.