ECL: Emitter-Coupled Logic

The key to reducing propagation delay in a bipolar logic family is to prevent a gate's transistors from saturating. Section BJT.3 shows how Schottky diodes can prevent saturation in TTL gates. However, it is also possible to prevent saturation by using a radically different circuit structure, called *current-mode logic (CML)* or *emitter-coupled logic (ECL)*.

current-mode logic (CML)

emitter-coupled logic (ECL)

Unlike the other logic families in this chapter, ECL does not produce a large voltage swing between the LOW and HIGH levels. Instead, it has a small voltage swing, less than a volt, and it internally switches current between two possible paths, depending on the output state.

The first ECL logic family was introduced by General Electric in 1961. The concept was later refined by Motorola and others to produce the still popular 10K and 100K ECL families. These families are extremely fast, offering propagation delays as short as 1 ns. The newest ECL family, ECLinPS (literally, ECL in picoseconds), offers maximum delays under 0.5 ns (500 ps), including the signal delay getting on and off of the IC package. Throughout the evolution of digital circuit technology, some type of ECL has always been the fastest technology for discrete, packaged logic components.

Still, commercial ECL families aren't nearly as popular as CMOS and TTL, mainly because they consume much more power. In fact, high power consumption made the design of ECL supercomputers, such as the Cray-1 and Cray-2, as much of a challenge in cooling technology as in digital design. Also, ECL has a poor speed-power product, does not provide a high level of integration, has fast edge rates requiring design for transmission-line effects in most applications, and is not directly compatible with TTL and CMOS. Nevertheless, ECL still finds its place as a logic and interface technology in very high-speed communications gear, including fiber-optic transceiver interfaces for gigabit Ethernet and Asynchronous Transfer Mode (ATM) networks.

ECL.1 Basic ECL Circuit

The basic idea of current-mode logic is illustrated by the inverter/buffer circuit in Figure ECL-1 on the next page. This circuit has both an inverting output (OUT1) and a noninverting output (OUT2). Two transistors are connected as a *differential amplifier* with a common emitter resistor. The supply voltages for this example are $V_{CC} = 5.0$, $V_{BB} = 4.0$, and $V_{EE} = 0$ V, and the input LOW and HIGH levels are defined to be 3.6 and 4.4 V. This circuit actually produces output LOW and HIGH levels that are 0.6 V higher (4.2 and 5.0 V), but this is corrected in real ECL circuits.

differential amplifier

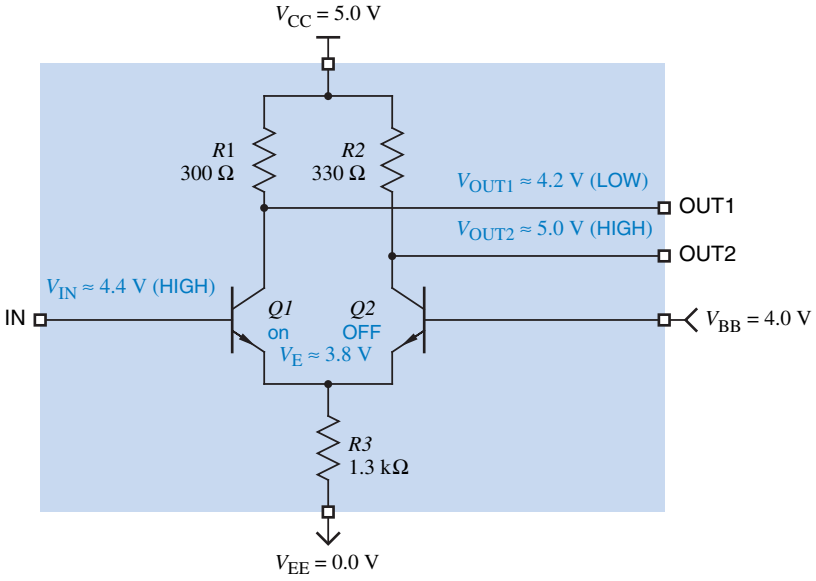


Figure ECL-1
Basic ECL inverter/ buffer circuit with input HIGH.

When V_{IN} is HIGH, as shown in the figure, transistor *Q1* is on, but not saturated, and transistor *Q2* is OFF. This is true because of a careful choice of resistor values and voltage levels. Thus, V_{OUT2} is pulled to 5.0 V (HIGH) through *R2*, and it can be shown that the voltage drop across *R1* is about 0.8 V, so that V_{OUT1} is about 4.2 V (LOW).

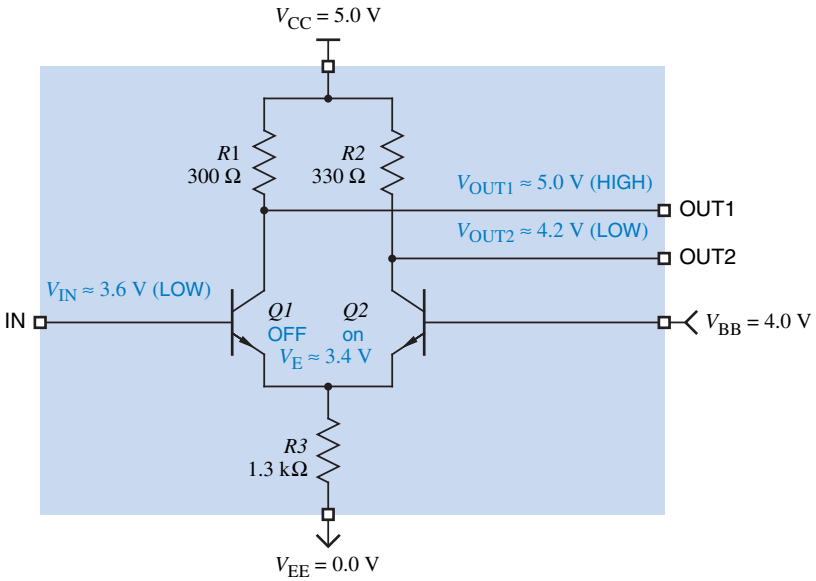


Figure ECL-2
Basic ECL inverter/ buffer circuit with input LOW.

When V_{IN} is LOW, as shown in Figure ECL-2, transistor *Q2* is on, but not saturated, and transistor *Q1* is OFF. Thus, V_{OUT1} is pulled to 5.0 V through *R1*, and it can be shown that V_{OUT2} is about 4.2 V.

differential outputs

The outputs of this inverter are called *differential outputs* because they are always complementary, and it is possible to determine the output state by looking at the difference between the output voltages ($V_{OUT1} - V_{OUT2}$) rather than their absolute values. That is, the output is 1 if ($V_{OUT1} - V_{OUT2}$) > 0, and it is 0 if ($V_{OUT1} - V_{OUT2}$) < 0. It is possible to build input circuits with two wires per logical input that define the logical signal value in this way; these are called *differential inputs*.

differential inputs

Differential signals are used in most ECL "interfacing" and "clock distribution" applications because of their low skew and high noise immunity. They are "low skew" because the timing of a 0-to-1 or 1-to-0 transition does not depend critically on voltage thresholds, which may change with temperature or between devices. Instead, the timing depends only on when the voltages cross over relative to each other. Similarly, the "relative" definition of 0 and 1 provides outstanding noise immunity, since noise created by variations in the power supply or coupled from external sources tends to be a *common-mode signal* that affect both differential signals similarly, leaving the difference value unchanged.

common-mode signal

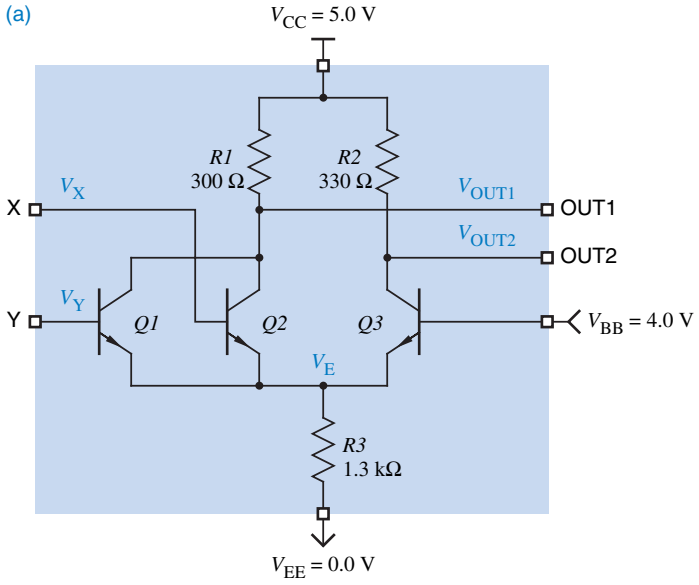
It is also possible, of course, to determine the logic value by sensing the absolute voltage level of one input signal, called a *single-ended input*. Single-ended signals are used in most ECL "logic" applications to avoid the obvious expense of doubling the number of signal lines. The basic ECL inverter in Figure ECL-2 has a single-ended input. It always has both "outputs" available internally; the circuit is actually either an inverter or a noninverting buffer, depending on whether we use OUT1 or OUT2.

single-ended input

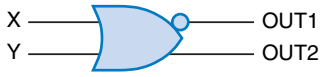
To perform logic with the basic circuit of Figure ECL-2, we simply place additional transistors in parallel with *Q1*, similar to the approach in a TTL NOR gate. For example, Figure ECL-3 on the next page shows a 2-input ECL OR/NOR gate. If any input is HIGH, the corresponding input transistor is active, and V_{OUT1} is LOW (NOR output). At the same time, *Q3* is OFF, and V_{OUT2} is HIGH (OR output).

Recall that the input levels for the inverter/buffer are defined to be 3.6 and 4.4 V, while the output levels that it produces are 4.2 and 5.0 V. This is obviously a problem. We could put a diode in series with each output to lower it by 0.6 V to match the input levels, but that still leaves another problem—the outputs have poor fanout. A HIGH output must supply base current to the inputs that it drives, and this current creates an additional voltage drop across *R1* or *R2*, reducing the output voltage (and we don't have much margin to work with). These problems are solved in commercial ECL families, such as the 10K family described next.

(a)



(c)



(b)

X	Y	V_X	V_Y	*Q1*	*Q2*	*Q3*	V_E	V_{OUT1}	V_{OUT2}	OUT1	OUT2
L	L	3.6	3.6	OFF	OFF	on	3.4	5.0	4.2	H	L
L	H	3.6	4.4	OFF	on	OFF	3.8	4.2	5.0	L	H
H	L	4.4	3.6	on	OFF	OFF	3.8	4.2	5.0	L	H
H	H	4.4	4.4	on	on	OFF	3.8	4.2	5.0	L	H

(d)

X	Y	OUT1	OUT2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Figure ECL-3 ECL 2-input OR/NOR gate: (a) circuit diagram; (b) function table; (c) logic symbol; (d) truth table.

ECL.2 ECL 10K/10H Families

ECL 10K family

The packaged components in today's most popular ECL family have 5-digit part numbers of the form "10xxx" (e.g., 10102, 10181, 10209), so the family is generically called *ECL 10K*. This family has several improvements over the basic ECL circuit described previously:

- An emitter-follower output stage shifts the output levels to match the input levels and provides very high current-driving capability, up to 50 mA per output. It is also responsible for the family's name, "emitter-coupled" logic.
- An internal bias network provides V_{BB} without the need for a separate, external power supply.

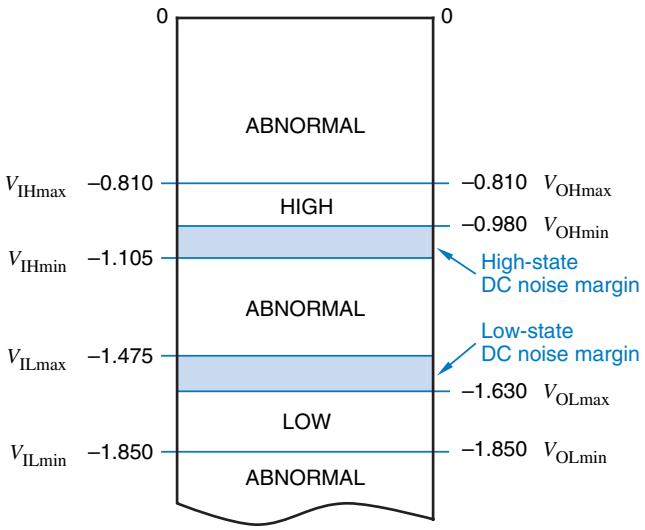


Figure ECL-4
ECL 10K logic levels.

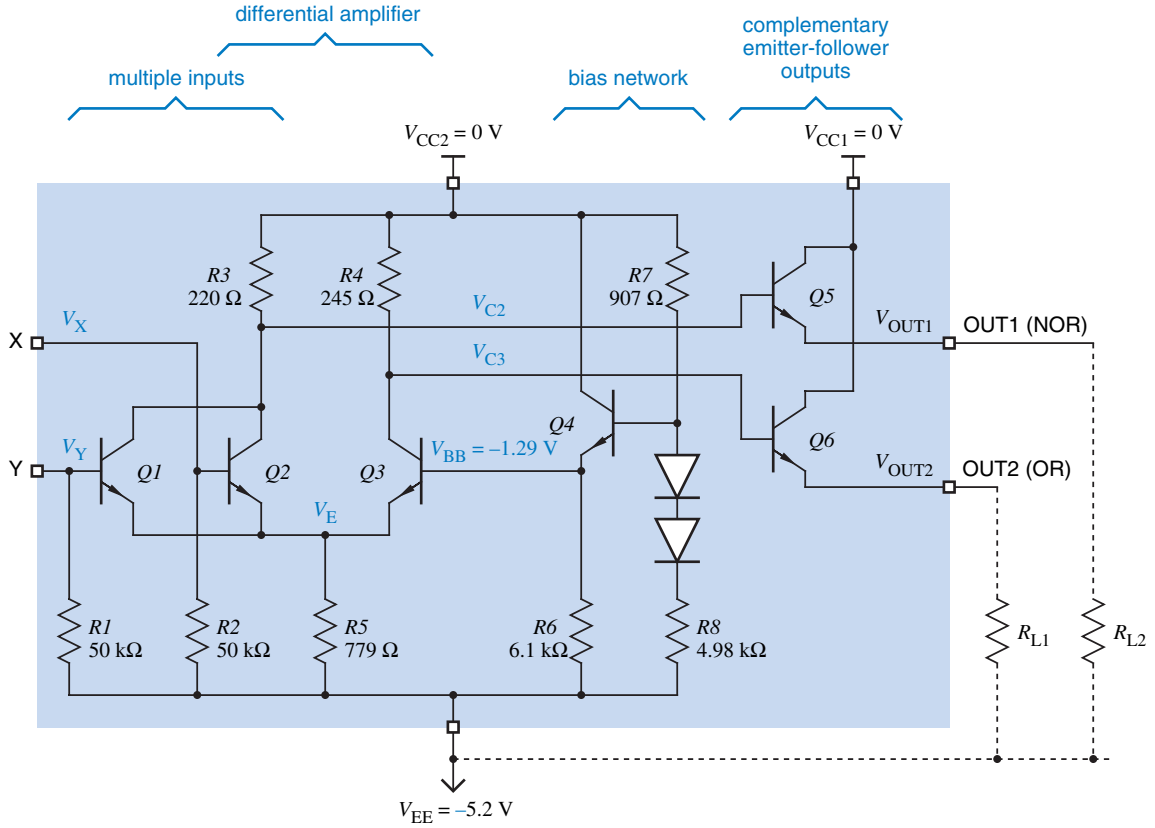
- The family is designed to operate with $V_{CC} = 0$ (ground) and $V_{EE} = -5.2$ V. In most applications, ground signals are more noise-free than the power-supply signals. In ECL, the logic signals are referenced to the algebraically higher power-supply voltage rail, so the family's designers decided to make that 0 V (the "clean" ground) and use a negative voltage for V_{EE}. The power-supply noise that does appear on V_{EE} is a "common-mode" signal that is rejected by the input structure's differential amplifier.
- Parts with a 10H prefix (the *ECL 10H family*) are fully voltage compensated, so they will work properly with power-supply voltages other than $V_{EE} = -5.2$ V, as we'll discuss in Section ECL.4.

ECL 10H family

Logic LOW and HIGH levels are defined in the ECL 10K family as shown in Figure ECL-4. Note that even though the power supply is negative, ECL still follows convention and assigns the names LOW and HIGH to the *algebraically* lower and higher voltages, respectively.

DC noise margins in ECL 10K are much less than in CMOS and TTL, only 0.155 V in the LOW state and 0.125 V in the HIGH state. However, ECL gates do not need as much noise margin as these families. Unlike CMOS and TTL, an ECL gate generates very little power-supply and ground noise when it changes state; its current requirement remains constant as it merely steers current from one path to another. Also, ECL's emitter-follower outputs have very low impedance in either state, and it is difficult to couple noise from an external source into a signal line driven by such a low-impedance output.

(a)



(b)

X	Y	V_X	V_Y	Q1	Q2	Q3	V_E	V_{C2}	V_{C3}	V_{OUT1}	V_{OUT2}	OUT1	OUT2
L	L	–1.8	–1.8	OFF	OFF	on	–1.9	–0.2	–1.2	–0.9	–1.8	H	L
L	H	–1.8	–0.9	OFF	on	OFF	–1.5	–1.2	–0.2	–1.8	–0.9	L	H
H	L	–0.9	–1.8	on	OFF	OFF	–1.5	–1.2	–0.2	–1.8	–0.9	L	H
H	H	–0.9	–0.9	on	on	OFF	–1.5	–1.2	–0.2	–1.8	–0.9	L	H

(c)

X	Y	OUT1	OUT2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

(d)

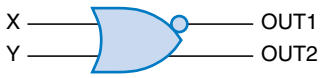


Figure ECL-5 Two-input 10K ECL OR/NOR gate: (a) circuit diagram; (b) function table; (c) truth table; (d) logic symbol.

Figure ECL-5(a) is the circuit for an ECL OR/NOR gate, one section of a quad OR/NOR gate with part number 10102. A pull-down resistor on each input ensures that if the input is left unconnected, it is treated as LOW. The bias network has component values selected to generate $V_{BB} = -1.29$ V for proper operation of the differential amplifier. Each output transistor, using the emitter-follower configuration, maintains its emitter voltage at one diode-drop below its base voltage, thereby achieving the required output-level shift. Figure ECL-5(b) summarizes the electrical operation of the gate.

The emitter-follower outputs used in ECL 10K require external pull-down resistors, as shown in the figure. The 10K family is designed to use external rather than internal pull-down resistors for good reason. The rise and fall times of ECL output transitions are so fast (typically 2 ns) that any connection longer than a few inches must be treated as a transmission line and must be terminated as discussed in Section Zo. Rather than waste power with an internal pull-down resistor, ECL 10K allows the designer to select an external resistor that satisfies both pull-down and transmission-line termination requirements. The simplest termination, sufficient for short connections, is to connect a resistor in the range of 270 Ω to 2 kΩ from each output to V_{EE}.

A typical ECL 10K gate has a propagation delay of 2 ns, comparable to 74AS TTL. With its outputs left unconnected, a 10K gate consumes about 26 mW of power, also comparable to a 74AS TTL gate, which consumes about 20 mW. However, the termination required by ECL 10K also consumes power, from 10 to 150 mW per output depending on the type of termination circuit. A 74AS TTL output may or may not require a power-consuming termination circuit, depending on the physical characteristics of the application.

ECL.3 ECL 100K Family

ECL 100K family

Members of the *ECL 100K family* have 6-digit part numbers of the form "100xxx" (e.g., 100101, 100117, 100170), but in general their functions are different from those of 10K parts with similar numbers. The 100K family has the following major differences from the 10K family:

- Reduced power-supply voltage, $V_{EE} = -4.5$ V.
- Different logic levels, as a consequence of the different supply voltage.
- Shorter propagation delays, typically 0.75 ns.
- Shorter transition times, typically 0.70 ns.
- Higher power consumption, typically 40 mW per gate.

ECL.4 Positive ECL (PECL)

We described the advantage of noise immunity provided by ECL's negative power supply (V_{EE} = −5.2 V or −4.5 V), but there's also a big disadvantage—today's most popular CMOS and TTL logic families, ASICs, and microprocessors all use a positive power-supply voltage, typically +5.0 V but trending to +3.3 V. Systems incorporating both ECL and CMOS/TTL devices therefore require two power supplies. In addition, interfacing between standard, negative ECL 10K or 100K logic levels and positive CMOS/TTL levels requires special level-translation components that connect to both supplies.

positive ECL (PECL)

Positive ECL (*PECL*, pronounced "peckle") uses a standard +5.0-V power supply. Note that there's nothing in the ECL 10K circuit design of Figure ECL-5 that requires V_{CC} to be grounded and V_{EE} to be connected to a −5.2-V supply. The circuit will function exactly the same with V_{EE} connected to ground, and V_{CC} to a +5.2-V supply.

Thus, PECL components are nothing more than standard ECL components with V_{EE} connected to ground and V_{CC} to a +5.0-V supply. The voltage between V_{EE} and V_{CC} is a little less than with standard 10K ECL and more than with standard 100K ECL, but the 10H-series and 100K parts are voltage compensated, designed to still work well with the supply voltage being a little high or low.

Like ECL logic levels, PECL levels are referenced to V_{CC}, so the PECL HIGH level is about V_{CC} − 0.9 V, and LOW is about V_{CC} − 1.7 V, or about 4.1 V and 3.3 V with a nominal 5-V V_{CC}. Since these levels are referenced to V_{CC}, they move up and down with any variations in V_{CC}. Thus, PECL designs require particularly close attention to power-distribution issues, to prevent noise on V_{CC} from corrupting the logic levels transmitted and received by PECL devices.

Recall that CML/ECL devices produce differential outputs and can have differential inputs. A differential input is relatively insensitive to the absolute voltage levels of an input-signal pair, and sensitive only to their difference. Therefore, differential signals can be used quite effectively in PECL applications to ease the noise concerns raised in the preceding paragraph.

It is also quite common to provide differential PECL-compatible inputs and outputs on CMOS devices, allowing a direct interface between the CMOS device and a device such as a fiber-optic transceiver that expects ECL or PECL levels. In fact, as CMOS circuits have migrated to 3.3-V power supplies, it has even been possible to build PECL-like differential inputs and outputs that are simply referenced to the 3.3-V supply instead of a 5-V supply.