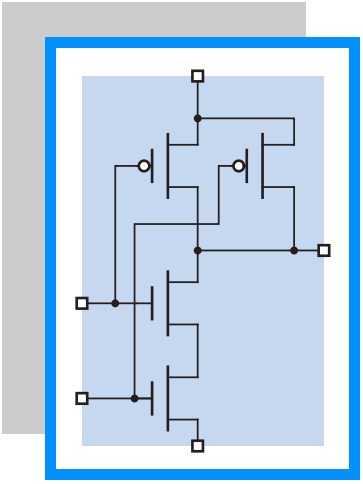


3

DIGITAL CIRCUITS

EXERCISE SOLUTIONS

3.1 The "probably" cases may cause damage to the gate if sustained.

(a) 0 (b) 1 (c) 0 (d) undefined

(e) 1 (f) probably 1 (g) probably 0 (h) probably 0

3.3 A logic buffer is a non-linear amplifier that maps the entire set of possible analog input voltages into just two output votages, HIGH and LOW. An audio amplifier has a linear response over its specified operating range, mapping each input voltage into an output voltage that is directly proprtional to the input voltage.

3.6 From the *American Heritage Electronic Dictionary (AHED)*, copyright 1992 by Houghton Mifflin Company:

(1) A structure that can be swung, drawn, or lowered to block an entrance or a passageway.

(2) a. An opening in a wall or fence for entrance or exit. b. The structure surrounding such an opening, such as the monumental or fortified entrance to a palace or walled city.

(3) a. A means of access: the gate to riches. b. A passageway, as in an airport terminal, through which passengers proceed for embarkation.

(4) A mountain pass.

(5) The total paid attendance or admission receipts at a public event: a good gate at the football game.

(6) A device for controlling the passage of water or gas through a dam or conduit.

(7) The channel through which molten metal flows into a shaped cavity of a mold.

(8) Sports. A passage between two upright poles through which a skier must go in a slalom race.

(9) Electronics. A circuit with multiple inputs and one output that is energized only when a designated set of input pulses is received.

Well, definition (9) is closest to one of the answers that I had in mind. The other answer I was looking for is the gate of a MOS transistor.

3.14 A CMOS inverting gate has fewer transistors than a noninverting one, since an inversion comes "for free."

3.15 Simple, inverting CMOS gates generally have two transistors per input. Four examples that meet the requirements of the problem are 4-input NAND , 4-input NOR , 2-in, 2-wide AND–OR–INVERT , and 2-in, 2-wide OR–AND–INVERT.

3.18 One way is that a romance could be sparked, and the designers could end up with a lot less time to do their work. Another way is that the stray perfume in the IC production line could have contaminated the circuits used by the designers, leading to marginal operation, more debugging time by the deidicated designers, and less time for romance. By the way, the whole perfume story may be apocryphal.

3.20 Using the maximum output current ratings in both states, the HIGH-state margin is 0.69V and the LOW-state margin is 1.02V. With CMOS loads (output currents less than 20 μA), the margins improve to 1.349V and 1.25V, respectively.

3.21 The first answer for each parameter below assumes commercial operation and that the device is used with the maximum allowable (TTL) load. The number in parentheses, if any, indicates the value obtained under a lesser but specified (CMOS) load.

V_{OHmin} 3.84V (4.4V)

V_{IHmin} 3.15V

V_{ILmax} 1.35V

V_{OLmax} 0.33V (0.1V)

I_{Imax} 1μA

I_{OLmax} 4 mA (20 μA)

I_{OHmax} -4 mA (-20 μA)

3.22 Current is positive if it flows *into* a node. Therefore, an output with negative current is *sourcing* current.

3.23 The 74HC00 output drive is so weak, it's not good for driving much:

(a) Assume that in the LOW state the output pulls down to 0.33V (the maximum V_{OL} spec). Then the output current is $(5.0\text{V})/120\Omega = 41.7\text{mA}$, which is way more than the 4-mA commercial spec.

(b) For this problem, you first have to find the Thévenin equivalent of the load, or 148.5Ω in series with 2.25V . In the HIGH state, the gate must pull the output up to 3.84V, a difference of 1.59V across 148.5Ω, requiring 10.7 mA, which is out of spec. In the LOW state, we have a voltage drop of 2.25V – 0.33V across 148.5Ω, so the output must sink 12.9 mA, again out of spec.

3.24 (In the first printing, change "74FCT257T" to "74HC00.") The specification for the 74HC00 shows a maximum power-supply current of 10 μA when the inputs aree at 0 or 5V, but based on the discussion in Section 3.5.3 we would expect the current to be more when the inputs are at their worst-case values (1.35 or 3.15V). If we consider "nonlogic" input values, the maximum current will flow if the inputs are held right at the switching threshold, approximately $V_{CC}/2$.

3.26 (In the first printing, change "74FCT257T" to "74HC00.") Using the formulas on page 119, we can estimate that $R_{p(on)} = (5.0 - 3.84)/0.004 = 290\Omega$ or, using the higher value of V_{OHmin} in the spec, that $R_{p(on)} = (5.0 - 4.4)/0.00002 = 30\text{K}\Omega$. (The discrepancy shows that the output characteristic of this device is somewhat nonlinear.) We can also estimate $R_{n(on)} = 0.33/0.004 = 82.5\Omega$.

3.29 The purpose of decoupling capacitors is to provide the instantaneous power-supply current that is required during output transitions. Printed-circuit board traces have inductance, which acts as a barrier to current flow at high frequencies (fast transition rates). The farther the capacitor is from the device that needs decoupling, the larger is the instantaneous voltage drop across the connecting signal path, resulting in larger spike (up or down) in the device's power-supply voltage.

3.32 (a) 5 ns.

3.38 Smaller resistors result in shorter rise times for LOW-to-HIGH transitions but higher power consumption in the LOW state. Stated another way, larger resistors result in lower power consumption in the LOW state but longer rise times (more ooze) for LOW -to-HIGH transitions.

3.39 The resistor must drop $5.0 - 2.0 - 0.37 = 2.63\text{V}$ with 5mA of current through it. Therefore $r = 2.63/0.005 = 526\Omega$; a good standard value would be 510Ω.

3.41 (*The Secret of the Ooze*.) The wired output has only passive pull-up to the HIGH state. Therefore, the time for LOW-to-HIGH transitions, an important component of total delay, depends on the amount of capacitive loading and the size of the pull-up resistor. A moderate capacitive load (say, 100 pF) and even a very strong pull-up resistor (say, 150Ω) can still lead to time constants and transition times (15 ns in this example) that are longer than the delay of an additional gate with active pull-up.

3.42 The winner is 74FCT-T—48 mA in the LOW state and 15 mA in the HIGH state (see Table 3–8). TTL families don't come close.

3.46 n diodes are required.

3.49 For each interfacing situation, we compute the fanout in the LOW state by dividing I_{OLmax} of the driving gate by I_{ILmax} of the driven gate. Similarly, the fanout in the HIGH state is computed by dividing I_{OLmax} of the driving gate by I_{IHmax} of the driven gate. The overall fanout is the lower of these two results.

	Low-state		High-state		Overall	Excess	
Case	Ratio	Fanout	Ratio	Fanout	Fanout	State	Drive
74LS driving 74LS	$\frac{8\text{mA}}{0.4\text{mA}}$	20	$\frac{400\mu\text{A}}{20\mu\text{A}}$	20	20	none	
74LS driving 74S	$\frac{8\text{mA}}{2\text{mA}}$	4	$\frac{400\mu\text{A}}{50\mu\text{A}}$	8	4	HIGH	$200\mu\text{A}$

3.50 For the pull-down, we must have at most a 0.5-V drop in order to create a V_{IL} that is no worse than a standard LS-TTL output driving the input. Since $I_{\text{ILmax}} = 0.4\text{mA}$, we get $R_{\text{pd}} = 0.5/0.004 = 1250\Omega$ and $P_{pd} = V_{\text{IL}}^2/R_{\text{pd}} = (0.5)^2/1250 = 0.2\text{mW}$. (Alternatively, $P_{\text{pd}} = V_{\text{IL}}I_{\text{IL}} = 0.5 \cdot 0.0004 = 0.2\text{mW}$)
For the pull-up, we must have at most a 2.3-V drop in order to create a V_{IH} that is no worse than a standard LS-TTL output driving the input. Since $I_{\text{IHmax}} = 20\mu\text{A}$, we get $R_{\text{pu}} = 2.3/0.00002 = 115\text{k}\Omega$ and $P_{\text{pu}} = V_{\text{IH}}^2/R_{\text{pu}} = (2.3)^2/115000 = 0.046\text{mW}$. (Alternatively, we could have calculated the result as $P_{\text{pu}} = V_{\text{IH}}I_{\text{IH}} = 2.3 \cdot 0.00002 = 0.046\text{mW}$.) The pull-up dissipates less power.

3.52 The main benefit of Schottky diodes is to prevent transistors from saturating, which allows them to switch more quickly. The main drawback is that they raise the collector-to-emitter drop across an almost-saturated transistor, which decreases LOW -state noise margin.

3.55

				LOW-state			HIGH-state		
R_{VCC} (Ω)	R_{GND} (Ω)	V_{Thev} (V)	R_{Thev} (Ω)	$V_{\text{Thev}} - V_{\text{OL}}$ (V)	I_{OL} (mA)	OK?	$V_{\text{OH}} - V_{\text{Thev}}$ (V)	I_{OH} (μA)	OK?
470	—	5.0	470	4.5	9.57	no	<0	—	yes
330	470	2.9375	193.875	2.4375	12.57	no	<0	—	yes

3.56

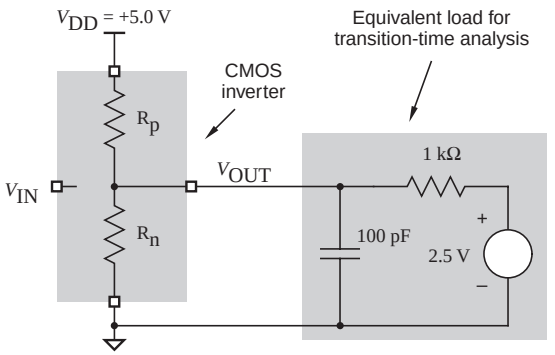
Case	LOW-state			HIGH-state		
	V_{ILmax}	$V_{OLmax(T)}$	Margin	V_{IHmin}	$V_{OHmin(T)}$	Margin
74HCT driving 74LS	0.8 V	0.33 V	0.47 V	2.0 V	3.84 V	1.84 V

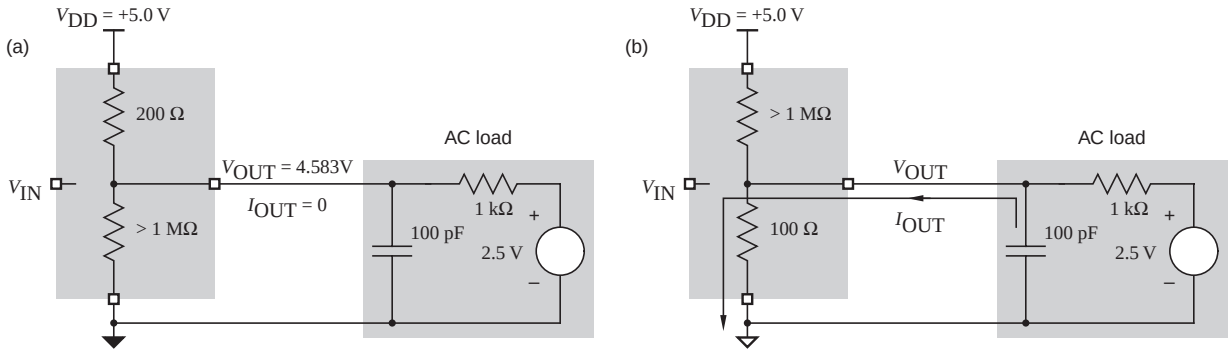
3.57 For each interfacing situation, we compute the fanout in the LOW state by dividing I_{OLmax} of the driving gate by I_{ILmax} of the driven gate. Similarly, the fanout in the HIGH state is computed by dividing I_{OHmax} of the driving gate by I_{ILmax} of the driven gate. The overall fanout is the lower of these two results.

Case	LOW-state		HIGH-state		Overall	Excess	
	Ratio	Fanout	Ratio	Fanout	Fanout	State	Drive
74HCT driving 74LS	$\frac{4\text{mA}}{0.4\text{mA}}$	10	$\frac{4000\ \mu\text{A}}{20\ \mu\text{A}}$	200	10	HIGH	3800 μA

3.64 TTL-compatible inputs have $V_{IHmin} = 2.0\,\text{V}$, and typical TTL outputs have $V_{OHmin} = 2.7\,\text{V}$. CMOS output levels are already high compared to these levels, so there's no point in wasting silicon to make them any higher by lowering the voltage drop in the HIGH state.

3.68 Including the DC load, a CMOS output's rise and fall times can be analyzed using the equivalent circuit shown to the right. This problem analyzes the fall time. Part (a) of the figure below shows the electrical conditions in the circuit when the output is in a steady HIGH state. Note that two resistors form a voltage divider, so the HIGH output is 4.583 V, not quite 5.0 V as it was in Section 3.6.1. At time $t = 0$ the CMOS output changes to the LOW state, resulting in the situation depicted in (b). The output will eventually reach a steady LOW voltage of 0.227 V, again determined by a voltage divider.





At time $t = 0$, V_{OUT} is still 4.583 V, but the Thévenin equivalent of the voltage source and the two resistors in the LOW state is 90.9 Ω in series with a 0.227-V voltage source. At time $t = \infty$, the capacitor will be discharged to the Thévenin-equivalent voltage and V_{OUT} will be 0.227 V. In between, the value of V_{OUT} is gov-

erned by an exponential law:

$$\begin{aligned} V_{OUT} &= 0.227\text{V} + (4.583 - 0.227\text{V}) \cdot e^{-t/(R_n C_L)} \\ &= 4.356 \cdot e^{-t/(90.9 \cdot 100 \cdot 10^{-12})}\text{V} \\ &= 4.356 \cdot e^{(-t)/(90.9 \cdot 10^{-9})}\text{V} \end{aligned}$$

Because of the DC load resistance, the time constant is a little shorter than it was in Section 3.6.1, at 9.09 ns. To obtain the fall time, we must solve the preceding equation for V_{OUT} = 3.5 and V_{OUT} = 1.5, yielding

$$t = -9.09 \cdot 10^{-9} \cdot \ln\frac{V_{OUT}}{4.356}$$

$$t_{3.5} = 1.99 \text{ ns}$$

$$t_{1.5} = 9.69 \text{ ns}$$

The fall time t_f is the difference between these two numbers, or 7.7 ns. This is slightly shorter than the 8.5 ns result in Section 3.6.1 because of the slightly shorter time constant.

3.70 The time constant is $1\text{k}\Omega \cdot 50\text{ pF} = 50\text{ ns}$. We solve the rise-time equation for the point at which V_{OUT} is 1.5 V, as on p. 118 of the text:

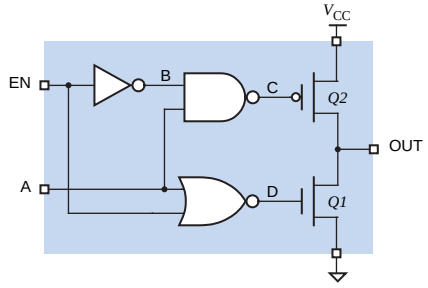
$$t_{1.5} = -50 \cdot 10^{-9} \cdot \ln\frac{5.0 - 1.5}{5.0}$$

$$t_{1.5} = 17.83 \text{ ns}$$

3.77 The LSB toggles at a rate of 16 MHz. It takes two clock ticks for the LSB to complete one cycle, so the transition frequency is 8 MHz. The MSB's frequency is 2^7 times slower, or 62.5 KHz. The LSB's dynamic power is the most significant, but the sum of the transitions on the higher order bits, a binary series, is equivalent to almost another 8 MHz worth of transitions on a single output bit. Including the LSB, we have almost 16 MHz, but applied to the load capacitance on just a single output. If the different ouputs actually have different load capacitances, then a weighted average would have to be used.

3.81

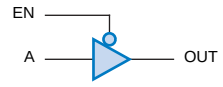
(a)



(b)

EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	H	on	off	L
L	H	H	L	L	off	on	H
H	L	L	H	L	off	off	Hi-Z
H	H	L	H	L	off	off	Hi-Z

(c)



3.84 In the situations shown in the figure, the diode with the lowest cathode voltage is forward biased, and the anode (signal C) is 0.6V higher. However, under the conditions specified in the exercise, neither diode is forward biased, no current flows through R_2, and V_C is 5.0V.

3.85

```
/* Transistor parameters */
#define DIODEDROP 0.6   /* volts */
#define BETA 10;
#define VCE_SAT 0.2     /* volts */
#define RCE_SAT 50      /* ohms  */
#define MAX_LEAK 0.00001 /* amperes */

main()
{
    float Vcc, Vin, R1, R2;  /* circuit parameters */
    float Ib, Ic, Vce;       /* circuit conditions */

    if (Vin < DIODEDROP) {   /* cut off */
       Ib  = 0.0;
       Ic  = Vcc/R2;  /* Tentative leakage current, limited by large R2 */
       if (Ic > MAX_LEAK) Ic = MAX_LEAK;  /* Limited by transistor */
       Vce = Vcc - (Ic * R2);
    }
    else {                   /* active or saturated */
        Ib = (Vin - DIODEDROP) / R1;
        if ((Vcc - ((BETA * Ib) * R2)) >= VCE_SAT) {   /* active */
            Ic  = BETA * Ib;
            Vce = Vcc - (Ic * R2);
        }
        else {               /* saturated */
           Vce = VCE_SAT;
           Ic  = (Vcc - Vce) / (R2 + RCE_SAT);
        }
    }
}
```

3.86 In order to turn on *Q2* fully, V_A must be 1.2 V , corresponding to the sum of the base-to-emitter drops of *Q2* and *Q5*. This could happen if both X and Y are 0.95 V or higher. In reality, a somewhat higher voltage is required, because the voltage divider consisting of *R1*, *R3*, and other components diverts current from the base of *Q2* from turning on fully until X and Y are about 1.1 V or higher (at 25 °C , according to the typical characteristics graphed in the TI TTL Data Book).

3.90 When the output is HIGH, the relay coil will try to pull it to 12 volts. The high voltage will typically cause high current to flow through the output structure back into the 5-V supply and will typically blow up the output. Open-collector TTL outputs theoretically should not have this problem, but most are not designed to withstand the 12-V potential and transistor breakdown will occur. A few TTL open-collector devices are designed with “high-voltage outputs” to solve this problem.

3.92 $F = W \cdot X + Y \cdot Z$

W	X	Y	Z	G	F	W	X	Y	Z	G	F
0	0	0	0	1	0	1	0	0	0	1	0
0	0	0	1	1	0	1	0	0	1	1	0
0	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	1	1	0	1	1	0	1
0	1	0	0	1	0	1	1	0	0	0	1
0	1	0	1	1	0	1	1	0	1	0	1

W	X	Y	Z	G	F	W	X	Y	Z	G	F
0	1	1	0	1	0	1	1	1	0	0	1
0	1	1	1	0	1	1	1	1	1	0	1

3.96 When one module is driving HIGH and the other $n-1$ modules are output-disabled, each disabled module has a 74LS125 output sinking $20\ \mu A$ of leakage current. In addition, each of the n modules has a 74LS04 input sinking $20\ \mu A$ of leakage current. Thus, the total sink current is $(n-1+n)\cdot 20\ \mu A$. The 74LS125 can source 2.6 mA in the HIGH state, so we find

$$(n-1+n)\cdot 20\ \mu A \le 2.6 mA$$

$$n \le 65$$

When one module is driving LOW and the other $n-1$ modules are output-disabled, each disabled module has a 74LS125 output sourcing $20\ \mu A$ of leakage current. In addition, each of the n modules has a 74LS04 input sourcing 0.4 mA. Thus, the total source current is $(n-1))\cdot 20\ \mu A + n\cdot 0.4\ \mu A$. The 74LS125 can sink 24 mA in the LOW state, so we find

$$(n-1)\cdot 20 \mu A + n\cdot 0.4 mA \le 24 mA$$

$$n \le 57$$

Overall, we require $n \le 57$.